EXPERIMENTS ON SHORT LENGTH FIBER OPTIC DIGITAL COMMUNICATION LINK

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CERTIFICATE

This is to certify that the work on "EXPERIMENTS ON A SHORT LENGTH FIBER OPTIC DIGITAL COMMUNICATION LINK" has been carried out under my supervision and guidance and that this has not been submitted elsewhere for a degree.

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P. SHUKLA

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER I

INTRODUCTION

1.1 General:

In the next few years optical fiber communication is expected to come out of the experimental stage to commercial use. It has credentials like, low transmission loss (5 dB/km), E.M.I. and R.F.I immunity properties, light weight, small size, flexibility in its support and usefulness. Simultaneously with the advent of reliable and long life laser diodes, and detectors, better splicing arrangement, and manufacture of lower loss optical fibres, cables and connectors, the commerical use of this mode of communication is bound to take an edge over the conventional system. Future large scale networks of computer and microcomputers will be heavily dependent upon optical fibers. Major computer system manufactures like DEC, IBM, Burroughs, Hewlett-Packard etc., have already started using optical fiber short links for inter-package connections.

Light weight, high capacity and freedom from electromagnetic interferences make optical fibers attractive also for various military uses. Already its use in missile launch control has been reported [1] . In fighter aircraft kilometers of electrical cables of large weights can be replaced by light weight optical fibers, thus giving

aircraft more speed and better manoeuverability. Optical fibers having immunity towards weather conditions and EM interferences are also suitable for use in Naval surface ships and submarines.

In this chapter we describe briefly the different subsystems of a typical fibre optic digital communication system and give representative specifications of the optical subsystems.

1.2 Typical Fiber Optic Digital Communication System:

The block schematic of a typical fiber optic digital communication system is shown in Fig. 1.1. Broadly it can be divided into two parts, one part (shown inside the dotted lines) contains the optical fiber channel alongwith the associated opto-electronic devices. The other part includes well known electrical subsystems found in any conventional base band digital communication system. Like in any other communication system, the primary aim here also would be to transmit data at the maximum possible rate for a given performance criterion in terms of the probability of error in detection of data symbols (bit error rate). An obvious way of attempting this is to use good quality communication channel, i.e., the optical channel in the present case. But, if there is no choice available in this regard, as is so in our case, it becomes necessary to optimize the electrical

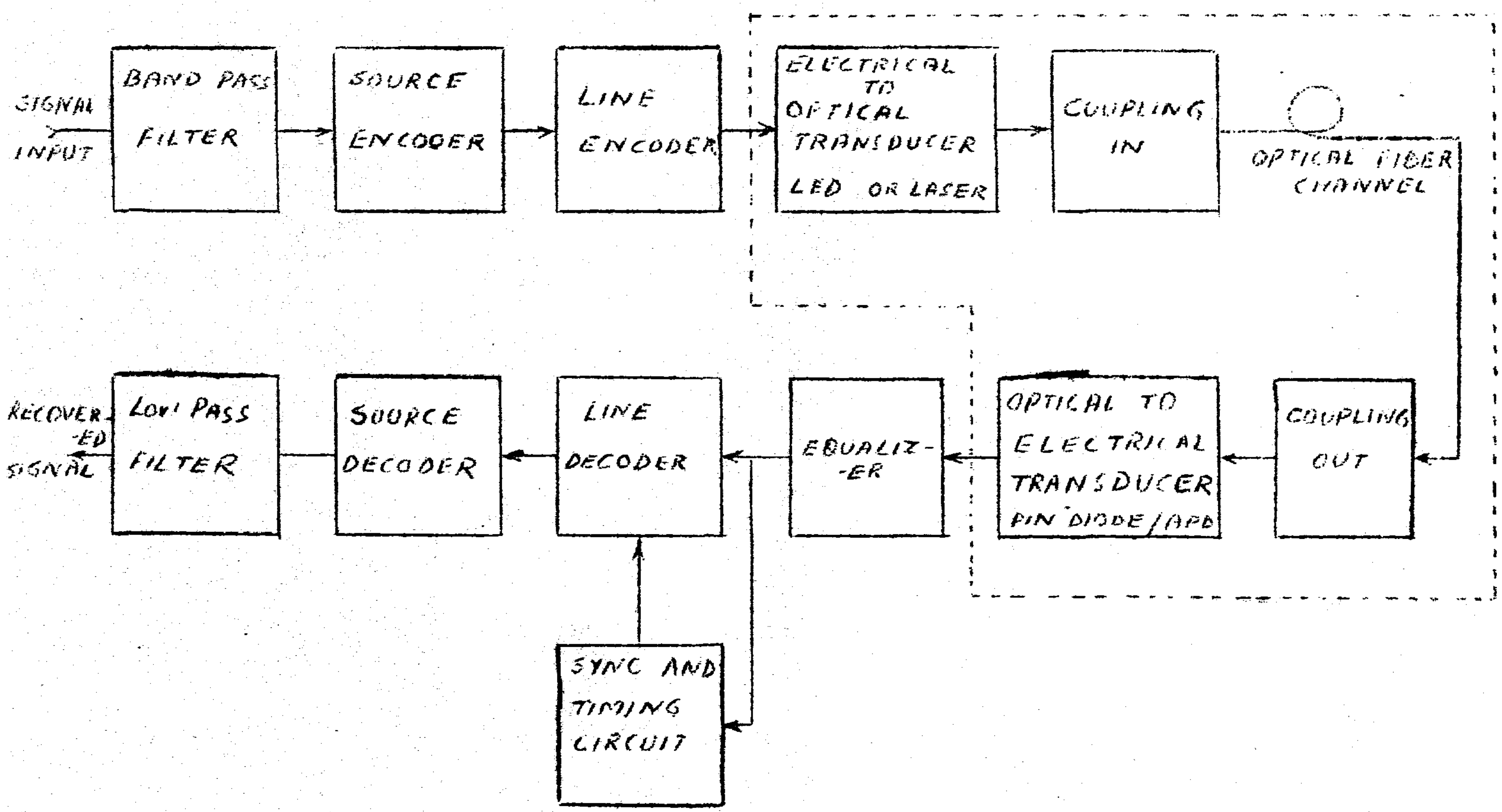

FIG 1.1 BLOCK DIAGRAM - FIBER OPTIC SYSTEM

portion for the best possible performance. For this purpose, both the electrical transmitter and the electrical receiver have to be efficiently designed. In the present study some attention has been paid to the possible choice of an efficient transmitter while using a conventional receiver.

1.2.1 Transmitter sub-systems:

The important subsystems at the transmitting end are the following;

i) Source Encoder
ii) Line Encoder
iii) Optical Source

i) Source Encoder:

Several efficient source coders are known, viz., PCM, DPCM, DM and the adaptive versions of the same. Out of these, only PCM seems to have been used as a source coder in the fibre optic digital communication systems reported so far. But, it is well known that DPCM and DM and their adaptive versions have some definite advantages over PCM. For this reason, DM and a modified form of it have been used as source encoders here.

ii) Line Encoder:

The need for line encoding arises because the conventional straight binary format has the following limitations;

(I) It can not provide an error monitoring capability.

(II) It suffers from occasional timing information disappearance.

(III) It can have a large dc content and thus result in a base line wander.

Other factors which necessitate line encoding and influence the selection are non linearity of the available optical sources like laser diodes, tolerance to intersymbol interference (ISI), bandwidth and optimum power requirements. The base band frequency spectrum must be relatively confined and have a null at zero frequency. This provides lower noise and permits ac coupling in the receiver. Some efficient line codes, known as mBnB pulse formats, have been shown to reduce such problems considerably. One of these pulse formats (2B3B) has been used as the line encoder here.

iii) Optical Source (Transducers):

Light sources for fiber optic communications systems requires certain characteristics including long life-time-in-use, high efficiency, reasonably low cost, sufficient power output, capability for various types of modulation and physical compatibility with fiber ends. The light sources that meet these requirements are semiconductor light emitting diodes (LEDs) and the semiconductor injection lasers.

Laser can launch more power in general, into low numerical aperture (NA) fibers than LEDs. The power output from lasers however is rather temperature sensitive compared to LEDs. These emit light within the 0.8-0.9 μm and 1.0-1.1 μm wavelength ranges, which are the regions of interest at present where the transmission loss of the fiber is low. Typical important features of LED's and semiconductor lasers are given in Table 1.1 [2].

1.2.2 <u>The Receiver Sub-systems</u>:

The important receiver sub-systems are the following.

i) Photo detectors

ii) Front-end low-noise amplifier

iii) Equalizers

iv) Synchronization Circuits

i) <u>Photo detectors</u>:

For optical fiber systems mainly two types of photo detectors are used; PIN photo diodes and Avalanche photo diodes (APD). These semiconductor optical detectors must meet the requirement of sufficient bandwidth (speed of response), adding minimum amount of noise to the transmitted signal, peak sensitivity at the light source wavelength stability over changing external temperature, long life at reasonable cost. Typical important features of PIN photo detector and APD are given in Table 1.2 [2].

Light Sources Types	Output Power Range(mW)	Bandwidth Range (Mbps)	Spectral width (Ang.st.)	Life-time average (hours)	Emitter's Area Range(mm^{-2})	Axial Radiance ($W/sr\text{-}cm^2$)	Source rise-time (ns)
Large Area LEDs	1-7	10-40	350	$6x10^4$	1-10	0.1-0.5	10-100
Small Area LEDs	0.5-1.5	20-200	330	$5x10^4$	0.004-0.040	5-70	3-20
CW laser diode	3-40	30-900	20	$4x10^4$	0.002-0.005	10-200	0.1-2
Pulsed Laser diode	100-400	0.1	20	$3x10^4$	0.002-0.005	10-200	0.1-2

Table 1.2

Basic Detector Type	Sensing Diameter Area (mm^2)	Sensitivity at 1 MHz (dBm)	Responsivity at Peak λ_o (A/W)	Bias Voltage (V)	Dynamic Range (dB)	Maximum Data Rate (Mbps)	Life time Range (hours)	Rise Time (ns)	Peak λ_o Response (nm)
PIN	0.3-3	-58	0.4-0.7	10-100	60	1-2 GHz	10^4-$5x10^5$	1-5	870
APD	0.8-8	-70	10-70	250-350	20	90-150 MHz	10^4-$3x10^5$	2-5	880

ii) Front-end Low-noise amplifier:

The main feature in designing the front-end amplifier is to keep the noise from various sources, as low as possible at the output. The various sources of noise are thermal noise associated with biasing resistors, noise associated with amplifying transistors, noise resulting from leakage current in photodiodes, quantum or shot noise, noise due to dark current, etc.

Two different approaches have been used in designing the front-end amplifier. In the first, an a.c. coupled amplifier with a large input time constant has been used for low noise amplification. While in the second, a shunt feed back amplifier commonly referred to as a transimpedance amplifier has been used. The large time constant of the first kind introduces further dispersion on the received pulses, and thus requires subsequent equalization. The second kind requires a marginal increase in the signal power.

iii) Equalizers:

In optical fibres, as in other transmission channels, dispersion of transmitted pulses cause inter-symbol interference (ISI), and so equalization of received pulses is needed for increased data rates and repeater spacing. Both frequency domain (fixed and variable) and time domain

(linear and nonlinear) equalizers have been used for this purpose in experimental systems.

iv) <u>Synchronization Circuits</u>:

Synchronization is a necessity in fibre optic digital communication systems as it is so far any other synchronous transmission system. But, here the synchronization circuits must be as simple as possible so that the cost of the repeaters can be kept small. High 'Q', LC tuned circuits have been used for this purpose. Efficient line coding methods can reduce the problems of synchronization.

1.3 <u>The Optical Fiber</u>:

Optical fibers are mainly of three types; step index single mode, step index multimode, and graded index multimode. In single mode, the core is of a very small size ($\simeq$2 to 5 μm) which enables propagation of a single mode only. Dispersion is least in this type of fiber, as only one mode propagates. This type of fiber is more expensive as very high precision is required in drawing the fiber [2]. Splicing (jointing) is also a problem for this type of fibers.

The step index multimode fibers have core of larger size compared to single mode ($\simeq$ 60 to 70 μm) and allow transmission of more than one mode thus resulting in a larger dispersion. The typical fiber diameter is dictated primarily

by the strength requirement in single mode fiber and by electrical transmission requirement in step index multimode fibers.

In the graded index fiber there is a gradual (normally parabolic) variation in the refractive index along the radius, being maximum at the center. In this type of fiber rays focus at periodic positions along the length of the fiber. This compensates for the mode dispersion found in the step index although the dispersion is not as low as in the single mode fiber. Some typical parameters are given in Table 1.

1.4 Connectors and Splices:

A connector links one fiber to another or to repeaters or end-devices. Connectors are usually demountable from the rest of the fiber optic transmission systems. These have some sort of locking and aligning mechanism , and must introduce a minimum amount of insertion loss. A splice is a form of coupler that permanently joins two fibers or two fiber bundles. Signal attenuation in all these must be kept to a minimum by proper alignment and efficient jointing techniques.

1.5 Scope of Work:

A fiber optic communication system as shown in the block diagram (Fig. 1.1) was set up in the laboratory using

Parameters of some Typical Commercial Optical Fiber : 2

Manufacturer and Fiber ID number	Fiber material	Fiber diam (m)	Fiber atten. dB/km	Tensile strength Kg	Index profile	Max. length Km	N.A.	Bend Radius cm
Corning 1028	Silica	125	6	10	Step	10	0.18	2.5
Corning 1152	Silica	125	10	10	Graded	10	0.20	2.5
Bell North BNR 7-2-A	Silica	100	10	30	Step	0.5	.20	3.0
Bell North BNR 7-1-A	Silica	100	10	30	Graded	0.5	.22	3.0
Dupont PPX-P140R	Plastic	400	470	40	Step	1.0	-	0.1
I.T.T. GG-02-5	Silica	125	5	150	Graded	1.5	.25	0.5

HEWLETT PACKARD (HP) integrated optical transmitter and receiver modules type HFBR-1001 and HFBR-2001, respectively. A step index multimode 50meter long fiber optic cable type HFBR-3003 was used along with the compatible connectors. Chapter II gives a detailed description of the HP transmitter and receiver modules. Block encoders for line encoding of the type 1B-2B and 2B-3B along with block decoders of type 2B-1B and 3B-2B were designed and fabricated. Details for design of line encoder/decoder is given in Chapter III. A modified delta modulator, where the slope overload in the input signal is sensed and the step size adjusted accordingly was used as the source encoder. A decoder compatible with the source encoder is also designed and fabricated. Chapter IV gives the design details of the source encoder/decoder. The details of performance, measurements and results obtained for bit error rate and signal-to-noise ratio measurements are given in Chapter V. A brief discussion of the results and suggestions for further work are also included in this chapter.

CHAPTER II

HEWLETT PACKARD FIBER OPTICAL TRANSMITTER-FIBER-RECEIVER LINK

2.1 Introduction:

The HFBR-1001 fiber optic transmitter is an integrated electrical to optical transducer designed for digital data transmission over single fiber channel. A bipolar integrated circuit and a GaAsP LED source convert TTL level inputs to optical pulses at data rate from dc to 10 Mb/s having a non-return-to-zero (NRZ) pulse format. An integral optical connector on the module provides easy interfacing with the fiber. The optical cable used is a step index, glass-clad fiber surrounded by silicon coating buffer jacket, and tensile strength members. This combination is then covered by a scuff resistant outer jacket.

HFBR-2001 fiber optic receiver is an integrated optical to electrical transducer for reception of digital data over single fiber channel. A silicon PIN photo-detector and a bipolar integrated circuit convert optical pulses to TTL level outputs with an optical sensitivity of 0.8 μW, a dynamic range of 23 dB and data rates to 10 Mb/s NRZ. An integral optical connector on the module allows easy interfacing without problems of fiber-detector alignment.

2.2 Specifications:

The transmitter and the receiver can operate in

two different modes - internal (low) or external (high) mode. These modes are described in the next section. The specifications for the transmitter and the receiver are given in Table 2.1 and Table 2.2, respectively.

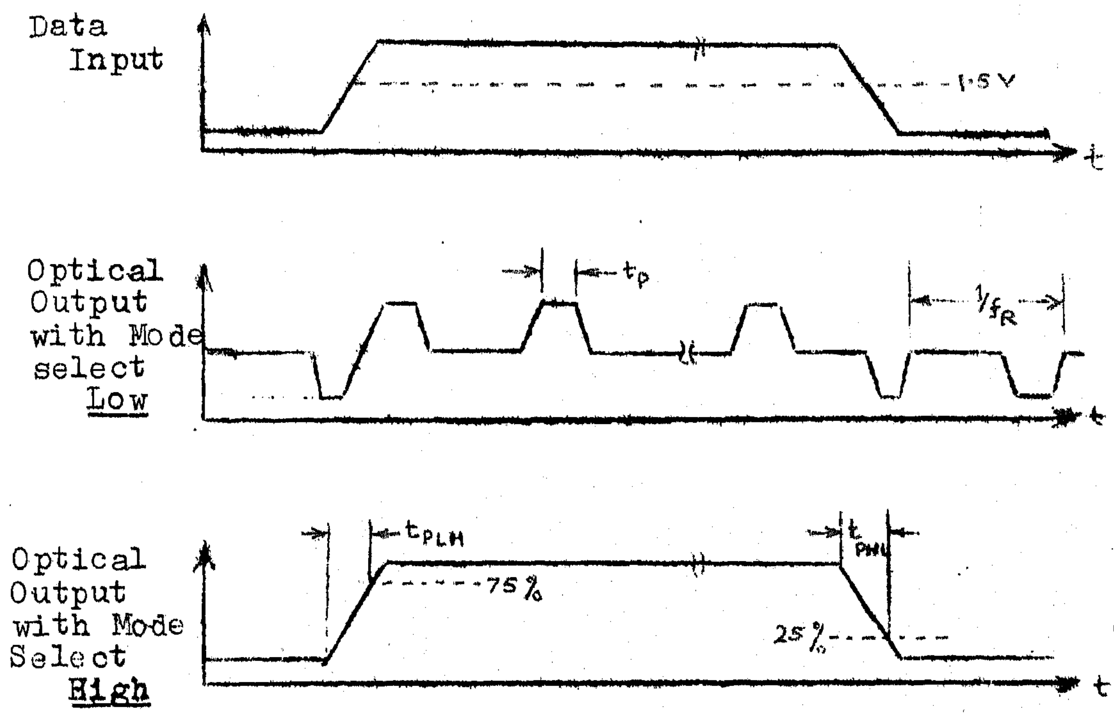

Fig. 2.1: Flux Coding and timing diagram.

2.3 Transmitter Description:

Fig. 2.2 shows symbolically the logic arrangement of the transmitter. To enhance the switching speed bias current I_C is never turned off in either internally - or externally coded mode. The three levels of flux viz low level (ϕ_L), mid level (ϕ_M) and high level (ϕ_H) are produced by current I_C, (I_B+I_C) and $(I_A+I_B+I_C)$, respectively. In the externally coded mode (mode select 'high') as shown in Fig. 2.1, the output flux is exact replica of the input

Table 2.1

OPTICAL TRANSMITTER SPECIFICATIONS

(1) Absolute Maximum ratings:

Parameter		Sumbol	Min.	Max.	Unit
Supply Voltage		V_{CC}	-0.5	6	V
Mode select or data input voltage		V_I	-0.5	5.5	V
Operating Temperature		T_A	0	70°	°C
Lead Soldering	Time			10	sec
	Temp			260	°C
Storage Temperature		T_S	-55	+85	°C

(2) Operating Conditions:

Supply Voltage	V_{CC}	4.75	5.25	V
High level input voltage Mode Select or Data input	V_{IH}	2.0	V_{CC}	V
Low level input voltage Mode select or Data input	V_{IL}	0	0.8	V
Data input Pulse Duration (high or low)	$t_H t_L$	100		ns
Ambient Temperature	T_A	0	70	°C

(3) Electrical/Optical Characteristics:

Exit Numerical Aperture (N.A.)		0.5
Coupling Losses(dB)	From Area Mismatch	6.0
	From N.A. Mismatch	4.0
Optical port (Fiber optic core)dia (μm)		200
Peak emission wavelength (nm)		700

Parameter	Mode select high		Mode select low		
	Data i/p high	Data i/p low	Mim.	Typ.	Max.
Supply Current (mA)	40	170	68	95	125
Optical flux 'Ø' (W)	67	3	-	35	-
Flux Excursion ratio (K)	depends on data format		0.8	-	1.2

(4) Dynamic Characteristics:

Parameter		Symbol	Min	Typ	Max
Propagation Delay (ns)	High to Low Data input step	t_{PHL}		31	45
Both modes	Low to high Data input step	t_{PLH}		35	50
Refresh Pulse Mode Select Low (internally coded mode)	Duration (ns)	t_p		60	
	Repetition Rate (KHz)	f_R		300	

Table 2.2

Optical Receiver Specifications

1) Optical Input pulse duration and timing:

Parameter		Symbol	Min.	Max.	Unit
2 level code	High level	t_H	100	5000	ns
	Low level	t_L	100	5000	
Flux Excursion Ratio		K	0.75	1.25	-
3 level code	High level	t_H	100	-	ns
	Low level	t_L	100	-	
	Mid level	t_M	100	-	
Refresh Repetition Rate		f_R	150	-	KHz
Refresh duty factor		$f_R t_H, f_R t_L$	-	0.04	-

2) Electrical/optical characteristic:

Parameter		Symbol	Min.	Typ.	Max.	Units
Data output voltage	High	V_{OH}	2.4	2.85	-	V
	Low	V_{OL}	-	0.35	0.5	V
Supply current		I_{CC}	60	77	100	mA
Numerical Aperture		N.A.	-	0.5	-	-
Peak responsivity wavelength		P	-	770	-	nm
High to low delay	3 level code	t_{PHL}	-	29	37	ns
	2 level code	t_{PHL}	-	37	35	ns
Low to high delay	3 level code	t_{PLH}	-	37	52	ns
	2 level code	t_{PLH}	-	45	60	ns
Bit Error Rase at 10M-band		BER	-	-	10^{-9}	-

The absolute maximum rating are same as given in Table 2.1.

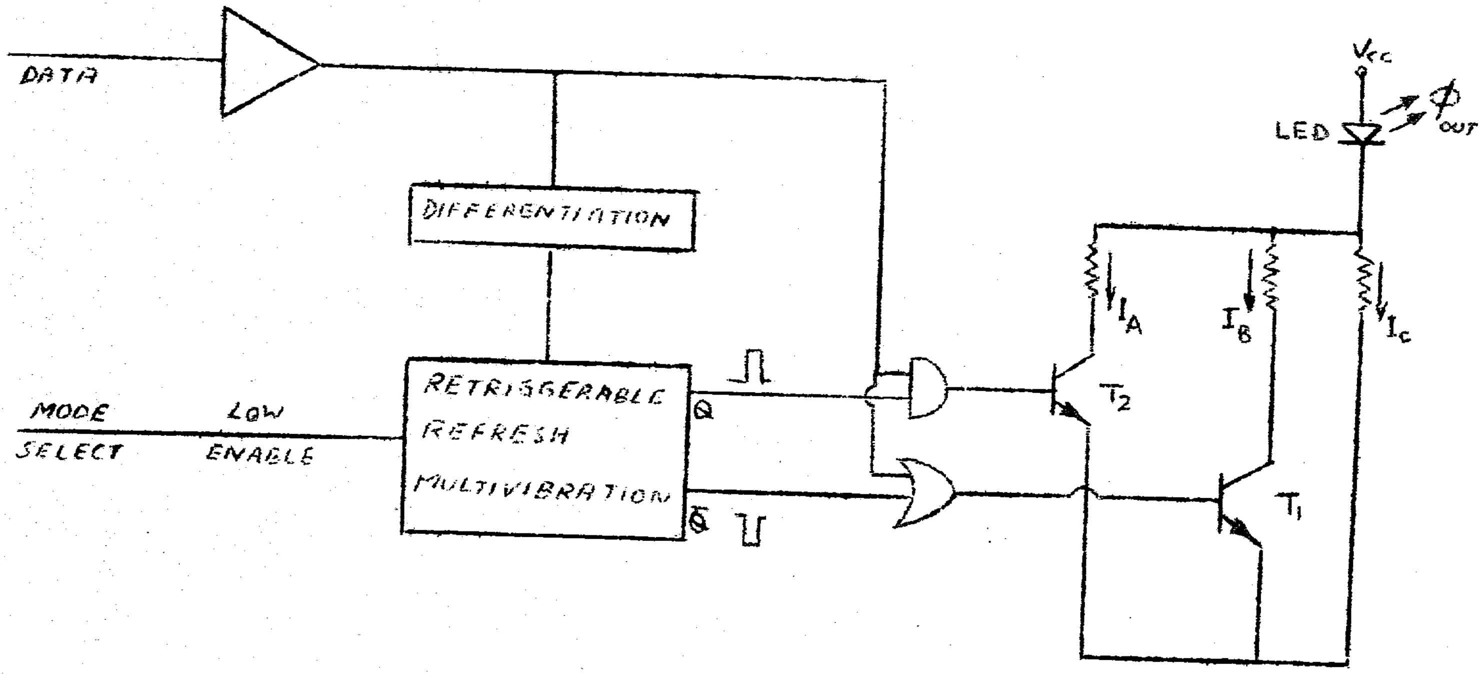

Fig 2.2. TRANSMITTER LOGIC DIAGRAM

signal. In this mode the Q output of the Refresh Multivibrator is 'high' (and $\bar{Q}$ is 'low'). Under this condition I_A and I_B are both ON when data input is 'high' and both OFF when it is 'low'.

In the internally coded mode (mode select 'low') the Refresh Multivibrator produces refresh pulses at pulse repetition frequency of 300 KHz and pulse duration of 60 ns (t_p). Any data transition (either H-L or L-H) retriggers the Refresh Multivibrator to start a new train of pulses. For data transition from Low to High refresh pulses from flux levels ϕ_M to ϕ_H are produced. For data transition from High to Low refresh pulses from flux levels ϕ_M to ϕ_L are produced. Notice that any refresh pulse is overridden by the occurrence of a data input transition so there is no additional jitter when the duration of the data input in either state is at or near the same length of time as the refresh interval. The refresh interval is very long, relative to the refresh pulse duration making a duty factor of about 2%. This also is done to keep the average flux near mid level regardless of how long data input remains in either logic state.

2.4 <u>Receiver Description</u>:

The receiver diagram is shown in Fig. 2.3, it has four functional blocks.

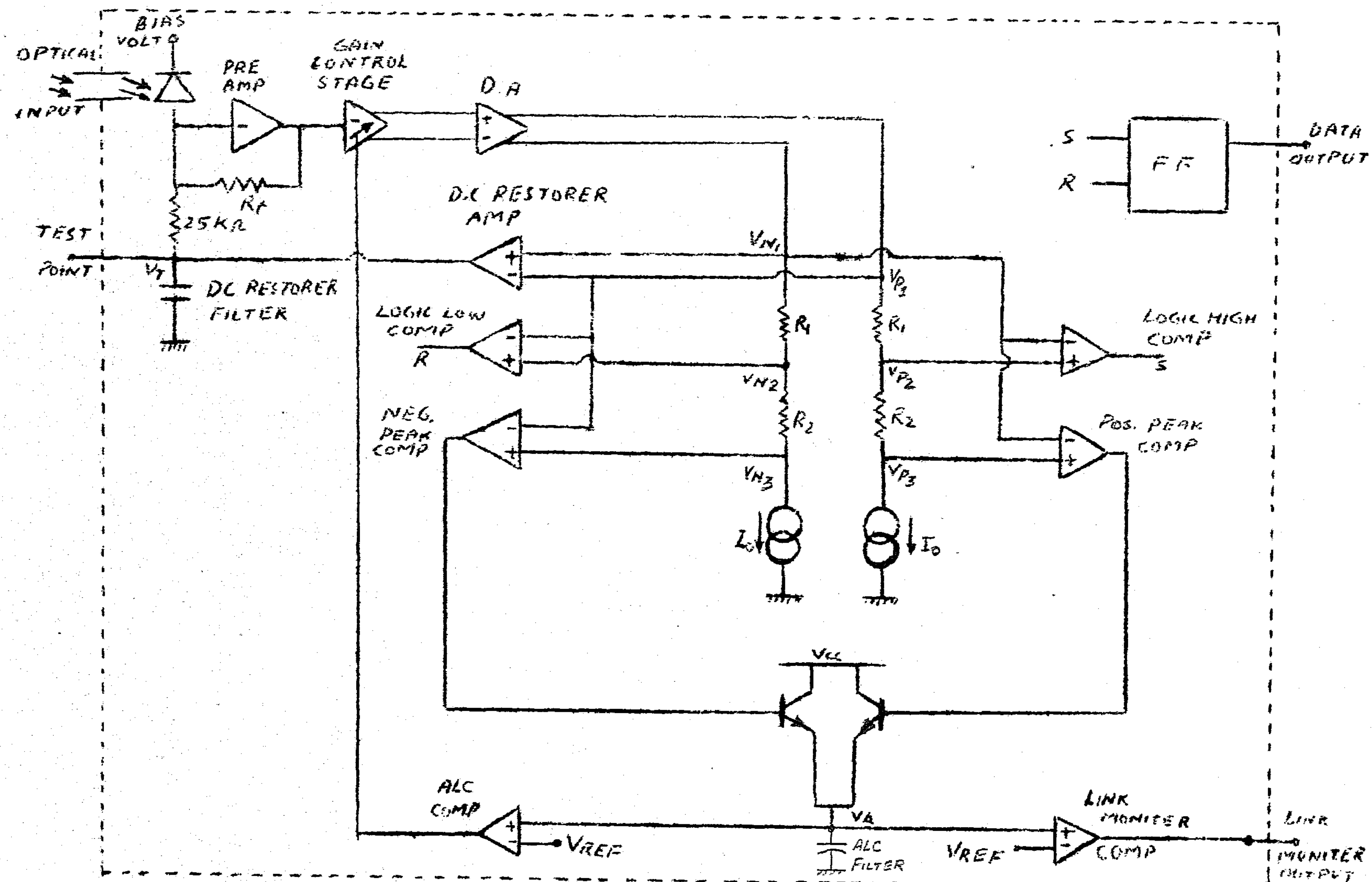

Fig: 23. RECEIVER DIAGRAM

i) The amplifier, including a gain-control stage and split phase outputs with a voltage devider for each.

ii) The d.c. restorer with a long time constant.

iii) Logic comparators with an R-S latch.

iv) Positive and negative peak comparator with single ended output for the ALC and link monitor circuit.

Optical flux at the input is converted by the PIN photodiode to a photocurrent I_P, which is converted to a voltage by the preamplifier. This voltage is amplified to a positive going output, V_{P1} , and a negative going output V_{N1}. A rising input flux will cause V_{P1} to rise and V_{N1} to fall. These voltages are applied to the differential inputs of the DC restorer amplifier whose output V_T falls until it is low enough to draw the average photocurrent away from the pre-amplifier via the 25K resistor. This makes $V_{P1} \simeq V_{N1}$ when the input flux is at the average level. The output impedance of the DC restorer amplifier is very high, making a long time constant with the filter capacitor, C_T. With no input flux $V_T = V^*_{max}$, as input flux rises, V_T falls proportionately, so that the voltage at the TEST POINT can be used as an indicator of the average input flux.

$^*V_{max}$ = Test point voltage with no optical input signal.

As described above, when this input flux is at the average level, the positive going and negative going output voltages V_{P1} and V_{N1} are approximately equal. Notice that this makes the outputs of both logic comparators low. A positive flux excursion, rising faster than the DC restorer can follow, will cause V_{P1} to rise and V_{N1} to fall. If the positive flux excursion is high enough, the logic High comparator input voltage $(V_{P2}-V_{N1})$ becomes positive and a SET pulse is produced for the R-S flip-flop. [Similarly, a negative flux excursion of such amplitude would make $(V_{N2}-V_{P1})$ positive and RESET pulse would be produced]Larger amplitude of positive flux excursion would make the Positive Peak Detector input voltage $(V_{P3}-V_{N1})$ change from negative to positive and cause current to flow into ALC filter capacitor. When voltage V_A starts to rise above V_{REF}, the ALC amplifier output will operate on the gain control amplifier to limit the receiver's forward gain. Notice that the ALC action is the same for a negative flux excursion.

2.5 Precautions and Limitations:

To be able to use the H.P. fiber optic link most efficiently and to save it from damaging following precautions are recommended. There are few important limitations in the use of link e.g. input data format etc. which are also mentioned below.

(i) Taking into considerations the transition time from L to H (or H to L) t_{PLH} (or t_{PHL}) which is specified as 50 ns maximum (Refer Sec. 2.2), the minimum pulse width for internal (low) or external (high) mode can be 100 ns. This implies that the maximum data rate in either mode possible is 10 Mbits/sec NRZ.

(ii) In the external mode input data format should be such that on an average the signal should have a 50% duty factor or make flux excursion ratio* (K) = 1 (allowed variation limits are $0.44 < \text{Duty factor} < 0.57$ or $0.75 < K < 1.25$). This is required to keep the average flux (ϕ_{av}) near mid level flux (ϕ_M) to avoid preamplifier stage from saturating and to make full use of its dynamic range. This is possible by choosing codes where total number of 'mark' interval is equal to the total number of 'space' intervals as in the Manchester code.

(iii) In the two level code (i.e. in the external code), the other requirement is that in either high or low level data should not remain for more than 5µ sec. This is

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*Flux excursion ratio (for internal mode-3 level code) $K \triangleq \dfrac{\phi_H - \phi_M}{\phi_M - \phi_L}$

Flux excursion ratio(for external mode-2 level code) $K \triangleq \dfrac{\Sigma\, t_L}{\Sigma\, t_H}$

(Fig. 2.1)

necessary to avoid "pulling" the receiver D.C. restorer voltage V_T too far away from the value corresponding to the average flux (Sec. 2.4). With this limitation in the external mode data rate less than 0.4 Mbits/sec can not be used even when a code like Manchester is used.

(iv) The instrument used for observing the voltage at test point V_T must not load the test point significantly, so an input resistance of 10 MΩ is recommended [3] .

(v) Power supply lines for the transmitter and the receiver should each have a pi-filter of two 60 µF shunt capacitors and a 2.2 µH ($< 1\Omega$) inductor. The transmitter needs this filter to prevent transient from reaching other equipment when LED currents are switched. The receiver needs the filter to keep line transients from interfering with its extremely sensitive amplifier. Receiver also needs regulated [3] supply to prevent low frequency transients or ripples from interfering with the data. π filter should be used between regulator and receiver supply terminals. Transmitter does not need any regulator if the supply voltage is in the specified range of 4.75 V to 5.25V (Sec. 2.2).

(vi) During the performance evaluation the equipments which are connected to the input of transmitter or at the output of receiver (e.g. Data generator type HP3760A and Error Detector type HP3761) should have proper impedance buffering.

(vii) The limits specified for the fiber and connector handling against the mechanical abuses, bending etc. should be observed. Moving the lock nut at the module connector can cause misalignment of the optical fiber stub inside the module resulting in a reduction of power output. Both transmitter and receiver modules should be mounted so that the lock nut at the optical port is not disturbed (overhanging the edge is recommended).

CHAPTER III

LINE ENCODING AND DECODING

3.1 Suitable Codes for Optical Fiber System:

In the conventional systems the line code used is Alternate Mark Inversion (AMI), i.e., the polarity of marks are inverted alternatively. Advantage of this code is that it has no d.c. content, and any violation of this indicates presence of error. Being three level code it is not suitable for the optical fiber system. But, to utilize the advantages of AMI coding plan a two level AMI is suggested [4].

3.1.1 Two Level AMI:

In this scheme the center level of AMI code is converted into two levels as shown in Figure 3.1 (b) and (c). The two possible 2 level AMI modes provide the redundancy and can be made use of for error detection. Clock recovery is easier, and decision threshold level is insensitive to input level variation. Optical power required does not depend on the pulse pattern. But, this method suffers from the disadvantage of requiring double the transmission bandwidth compared to AMI or straight binary.

3.1.2 Block Codes:

This coding scheme implies that a block of m bits are converted into a block of n bits in the same time interval with the help of some conversion rule. Such codes are called

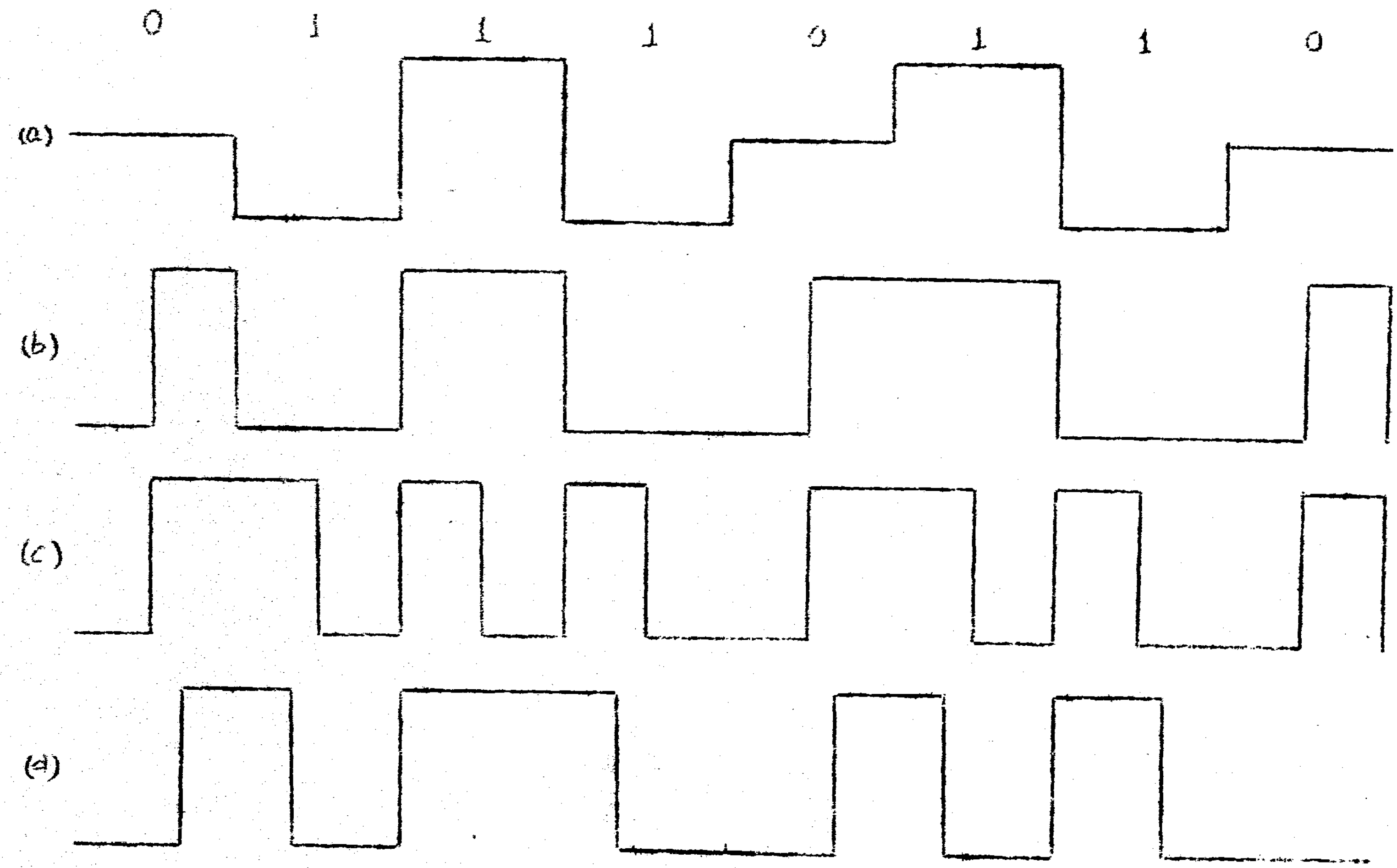


FIG 3.1 (a) CONVENTIONAL (THREE - LEVEL) AMI (d) 2B - 3B
(b) TWO LEVEL AMI CLASS - I
(c) TWO LEVEL AMI CLASS - II OR 1B - 2B

mB nB pulse formats. In general mB nB formats are suitable for optical transmission, if the ratios n/m is kept low. The bandwidth requirement can be minimized by keeping n=(m+1). Two block coders, for 1B 2B and 2B 3B, are described below.

a) <u>Coder 1B2B</u>:

The two-level AMI explained in Sec.3.1.1 can be termed as 1B2B code with the following conversion rule

Straight Binary	Mode 1	Mode 2	
1	11	-1,-1	Alternatively
0	1-1	-1, 1	Depends on the last bit of previous coded set.

The coding scheme could be made simpler by adopting the rule

1	1,0
0	0,1

The difference between the two being that former is converted from AMI and thus retains the pattern of AMI, whereas the latter is direct conversion from straight binary and can be considered as true 1B2B code (Also known as Manchester code).

Code convertor required for 1B2B is very simple as shown in the Fig. 3.2. Here data generator clock CK_2 is taken as divide by two clock from clock generator because it is easier to divide than multiply the clock. Behaviour of the circuit can be easily understood with the help of Fig. 3.2(b).

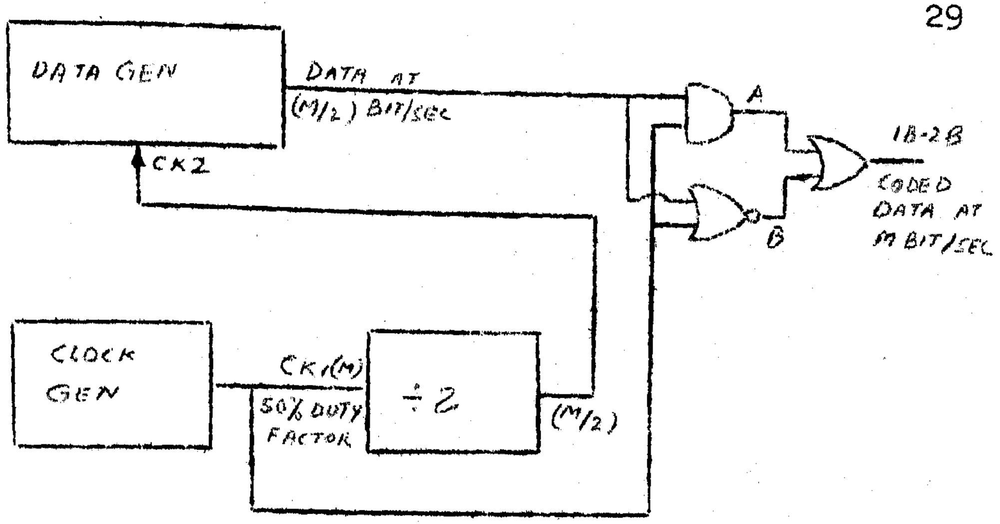


FIG. 3.2(a) CODER 1B-2B

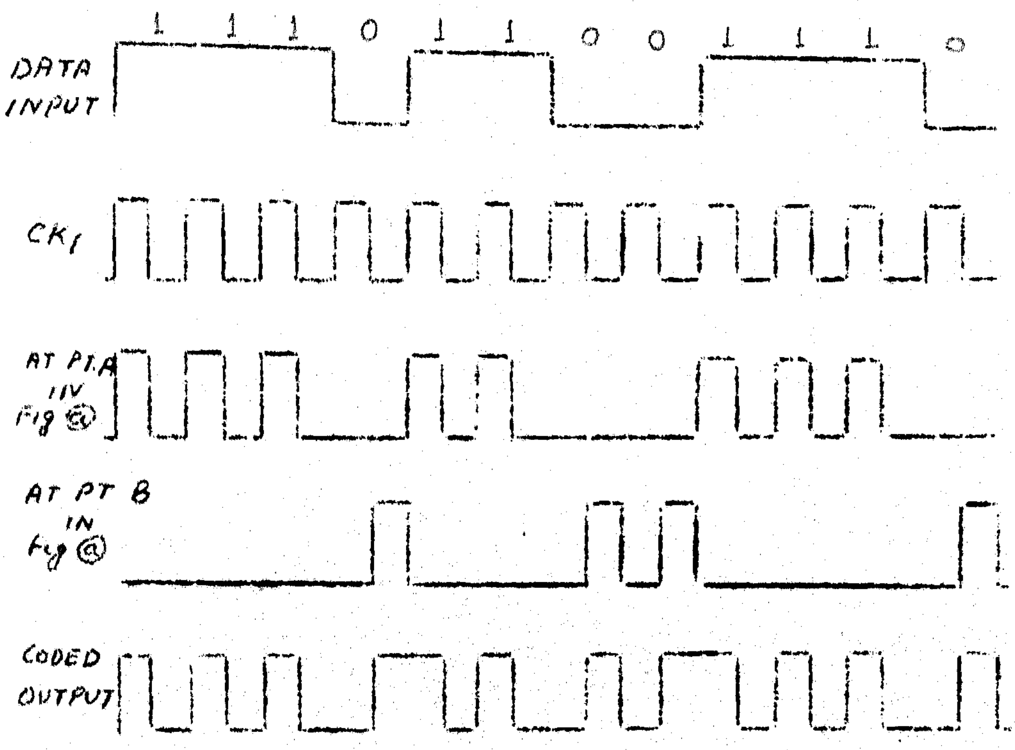


FIG 3.2 (b) WAVE FORMS CODER 1B-2B

b) Coder -2B-3B:

In 2B-3B coder data is accepted in 'block' of 2 bits and converted to blocks of 3 bits according to the rule given below in Table 3.1. As stated above the bandwidth saving can be done by reducing the conversion ratio n/m in mBnB type coders. For example, 2B3B format requires less bandwidth compared to 1B2B, as it includes less redundancy. However, the converter complexity increases exponentially as the redundancy is reduced [4] . So one has to strike a balance and select the code accordingly to fulfil the requirements and overcome the disadvantages of the straight binary plan.

Table 3.1

Original data X_1 X_0	2B3B code mode 1 Y_2 Y_1 Y_0	Mode 2
0 0	0 0 1	
0 1	0 1 0	
1 0	1 0 0	
1 1	1 1 0	0 0 0 alternately

Conventional 2B-3B plans try to suppress the dc component in a pulse sequence and as such can not solve the problem of error monitoring since the redundancy is used up in suppressing the dc component. Fig. 3.3 gives the block

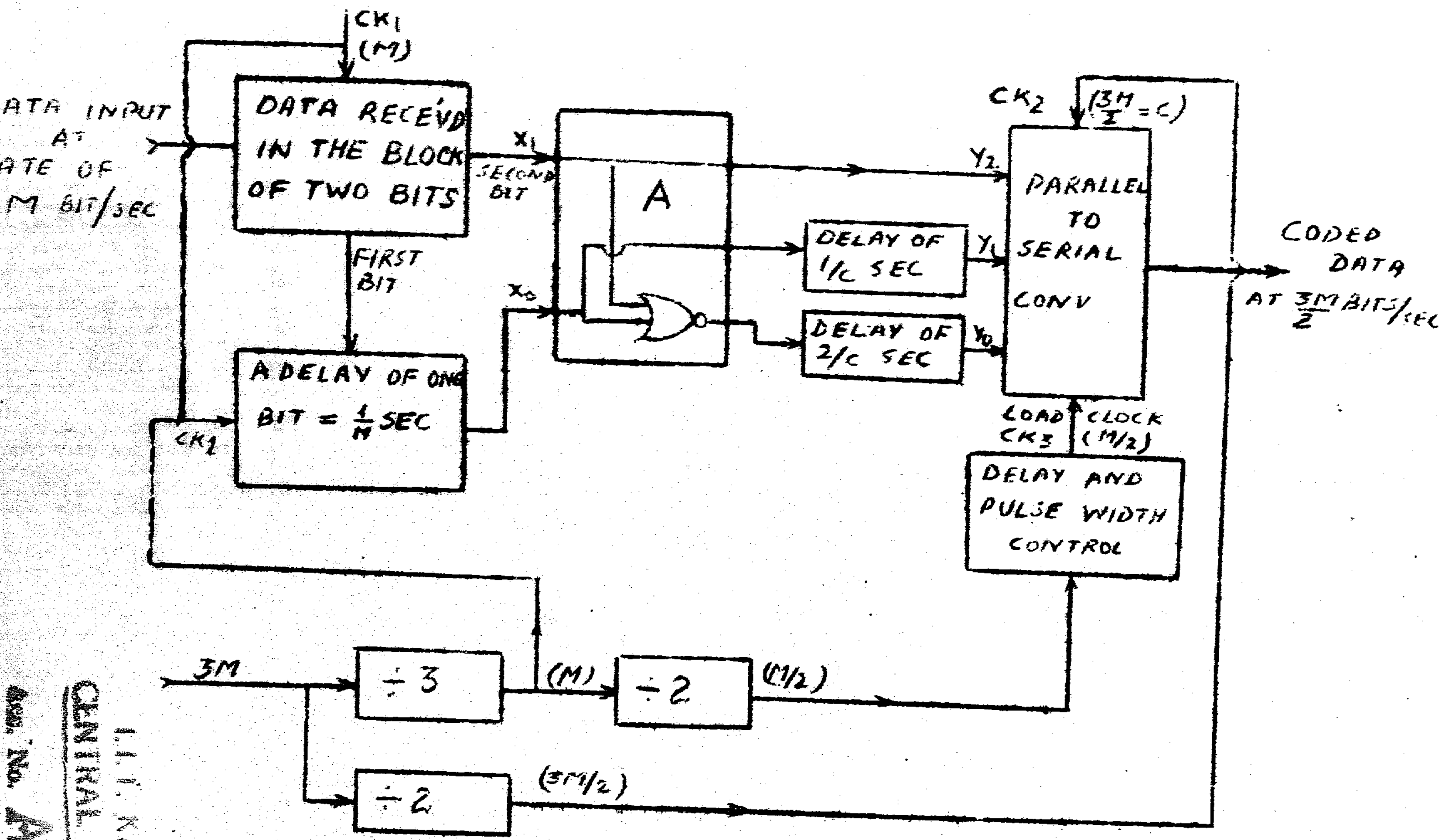
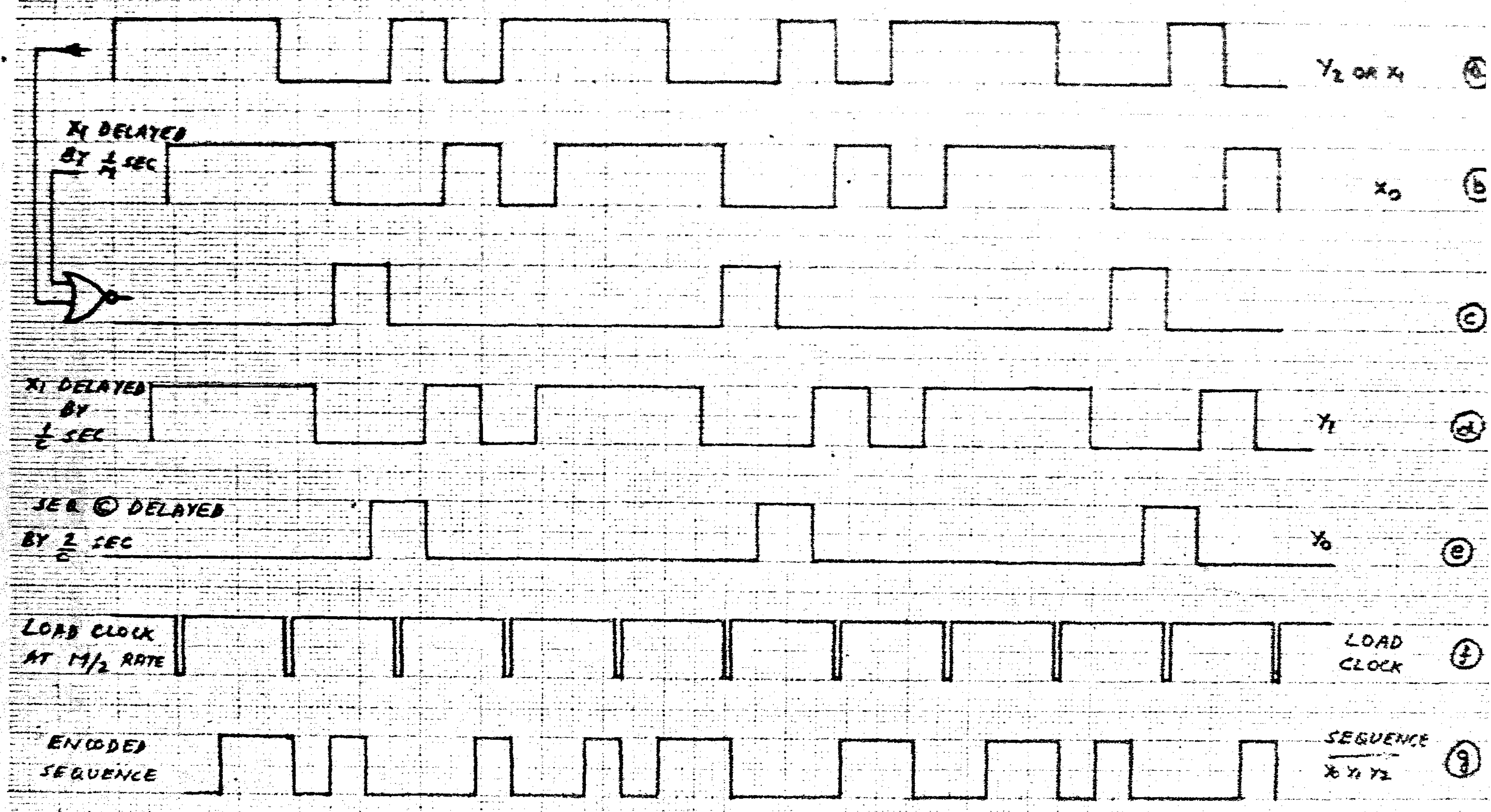


FIG 3.3 BLOCK DIAGRAM 2B - 3B CODER

schematic of the 2B-3B coder. In this the first bit of the data stream, after a delay of one bit duration is received as X_0 at the input of the block A. Whereas the second bit of the data stream is received as X_1 without any delay at the input of block A. Thus both first and second bits of the data stream are received simultaneously at the input of block A. The third bit of data stream is delayed by one bit duration again and received as X_0, while fourth bit without a delay is received again as X_1 at the inputs of block A. This way data bits are received in groups of two bits and available simultaneously at the input of block A. Block A is a simple digital circuit as shown and it converts the group of two bits in to group of 'three' bits according to the rule given in Table 3.1 mode 1. Notice here that these 'three' bits are to be transmitted in the time $\frac{2}{M}$ seconds (where M bits/sec is the rate of input data). These parallelly (simultaneously) available bits are to be transmitted in a serial order of $Y_2\ Y_1\ Y_0$. Therefore, bit Y_1 should come after a delay of $\frac{1}{3}\ (\frac{2}{M}) = \frac{1}{C}$ seconds (where $C = \frac{3M}{2}$, clock rate of transmission). Similarly bit Y_0 should come after a delay of $2 \times \frac{1}{C}$ seconds. A delay of T seconds can be provided by shift register 74164 by giving the clock of $\frac{1}{T}$ Hz to it. Fig. 3.4(a) shows the input data stream as X_1(a PRBS 2^N-1 for N=3). X_0 is the delayed sequence by one bit ($\frac{1}{M}$ sec) is shown in Fig. 3.4(b).



ⓐ INPUT DATA STREAM A PRBS 2^N-1 FOR $N=3$

ⓖ OUTPUT OF CODER 2B-3B WITH ABOVE INPUT

FIG 3.4 ; WAVE-FORMS IN CODER 2B-3B

Fig. 3.4(d) shows Y_1 which is delayed by $\frac{1}{C}$ sec $(= \frac{2}{3M})$. Fig. 3.4(e) is Y_0 delayed by $\frac{2}{C}$ sec $(= \frac{4}{3M}$ seconds).

For converting parallel data to serial output shift register 74165 was used. It requires a loading clock as shown in Fig. 3.4(f) at a rate $\frac{M}{2}$. With the arrival of this clock (at negative going edge) the fresh set of data is loaded to the shift register input which is transmitted one after the other. Thus loading clock should be available after $\frac{2}{M} + \Delta$ seconds. This Δ seconds delay is required so that full set of Y_2, Y_1, Y_0 should already be available when the loading clock edge arrives. This delay was kept approximately 80 n.sec (Four gate delay). Duration of clock (i.e. at 0V level) should also be very small compared to bit duration ($\frac{1}{C}$ sec). The encoded sequence is shown in Fig. 3.4(g) which is the output of coder.

Apart from the load clock discussed above three more clocks of rate M, $\frac{M}{2}$, $\frac{3M}{2}$ are required. These clocks are derived from the available clock from clock generator of rate 3M by successive division as shown in the Fig. 3.3. The division of clocks are preferred to multiplication as simple circuitry is required for division. Counters 74190 was used for dividing the clock.

3.2 Decoder 3B-2B:

Block schematic diagram is shown in Fig. 3.5. It is

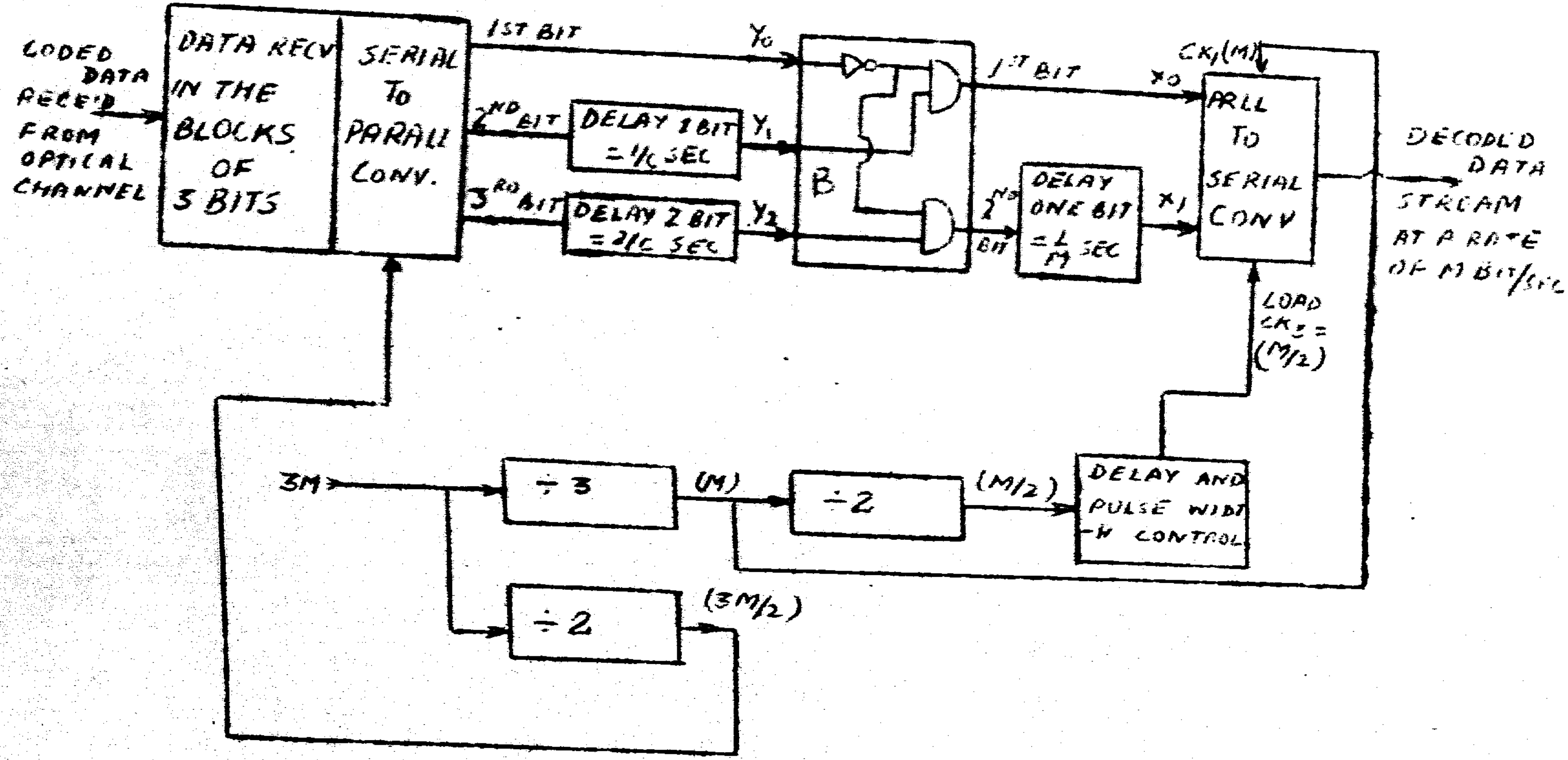


Fig 3.5 BLOCK DIAGRAM 3B-2B DECODER

designed on similar lines as the encoder. It is required here that coded data received here should be in blocks of three bits. Among these three bits the second and third bits are delayed by one bit ($\frac{2}{3}$M sec $= \frac{1}{C}$) and two bit ($\frac{2}{C}$) duration, respectively. Thus we notice that delay provided here is in the reverse order as was done in encoder i.e. bit Y_2 is delayed by two bit duration on ($\frac{2}{C}$ sec), bit Y_1 is delayed by one bit duration ($\frac{1}{C}$ sec) and bit Y_0 with no delay. Whereas at the encoder Y_0 was delayed by two bit duration ($\frac{2}{C}$ sec), Y_1 was delayed by one bit duration ($\frac{1}{C}$ sec) and Y_2 had been provided with no delay. Thus the over all delay for all data bits are ($\frac{2}{C}$ sec).

The simultaneously (parallelly) available bits Y_0, Y_1, Y_2 are converted to X_0 and X_1 with simple circuitry as shown in the block B, according to rule given in table 3.2. Before converting parallelly available X_1 and X_0 in to a serial output. Bit X_1 is to be delayed by one bit ($\frac{1}{M}$ sec), so that during loading clock edge in the parallel to serial convertor 74165, X_1 and X_0 are loaded as present and previous bits.

As explained in Sec. 3.1.2(b), here also the loading clock is similarly achieved. Also presuming that a clock

Table 3.2

Y_2	Y_1	Y_0	X_1	X_0
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	0	1	1

3M is available at the receiver. It is divided successively, as shown, to obtain the required clocks. A clock recovery and synchronization circuit was made using the PLL XR215, but it has a very narrow lock range around 2 MHz. For testing the circuit performance at other than this frequency variable clock generator was used. Results are given in the Chapter V.

CHAPTER IV

SOURCE CODER

4.1 Introduction:

Though PCM, DPCM, DM and the adaptive versions of the same are known source coders, but PCM is more commonly used in fiber optic communication systems. Compare to other coding scheme, hardware implementation of delta modulation (DM) being easy, linear delta modulation and a modified modified version of it have been used as source coder here.

4.2 Linear Delta Modulator:

Delta modulator acts as an analogue to digital convertor having an analogue input X(t) and a binary output signal L(t). The rate of occurence of each binary pulse is directly proportional to the instantaneous slope X(t). The step size is assumed to be a constant in Linear Delta Modulation (LDM) i.e. there is no modification done in step size in accordance with the changing slope of the input signal.

The block schematic of LDM is given in Fig. 4.1(a). The comparator inputs are the input signal and the sum of all previous samples. When the difference of these two

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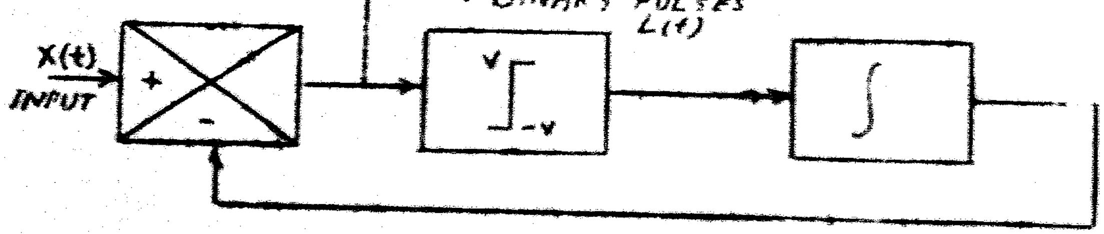

FIG 4·1 (a) LDM BLOCK DIAGRAM

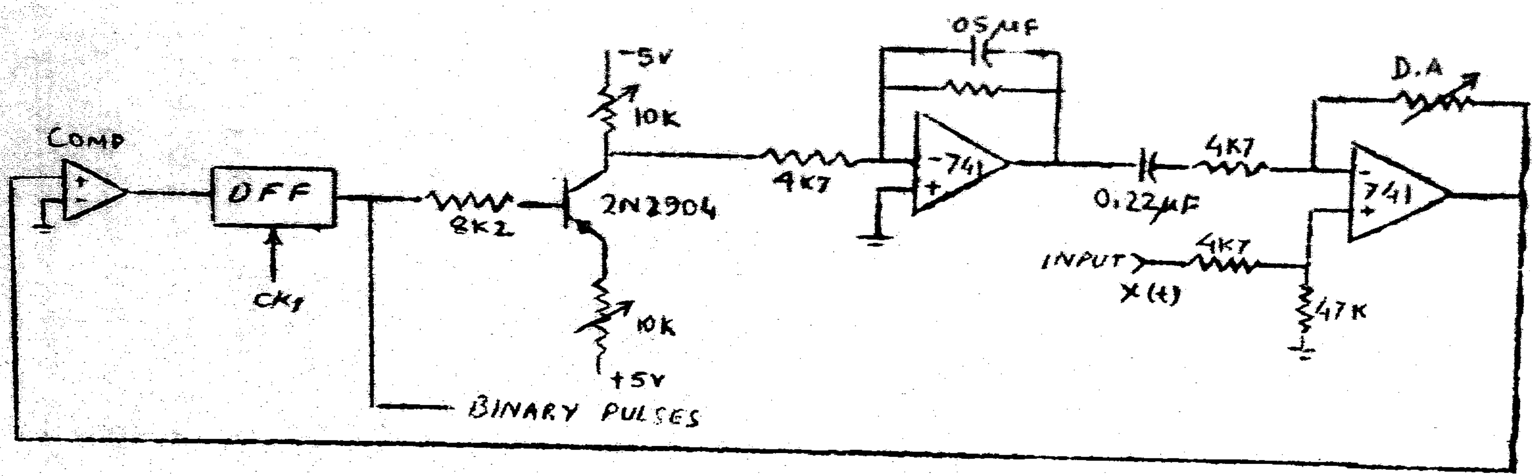

FIG 4·1 (b) CIRCUIT DIAGRAM – LDM

input increases more than a preset value (step size), the comparator gives a binary output. These binary pulses are level shifted before summing in an integrator.

Fig. 4.1(b) shows the circuit diagram of LDM. The output of the comparator is fed to the DFF to get the signal synchronized with the clock. TTL output (0-5V) is summed in the integrator after level shifting (-5V to 5V) with transistor 2N2904. The difference amplifier (DA) is designed to amplify the difference between incoming signal X(t) and the feed back signal Y(t) through local decoder such that error signal e_r always remains greater than five millivolts to get the binary output from the comparator.

4.3 <u>Types of Error in DM</u>:

There are two types of error found in delta modulation system.

i) Slope overload noise
ii) Granular noise

i) <u>Slope overload noise</u>: If K is the step size and T is the sampling period in seconds, then $\frac{K}{T}$ will be the highest input rate of change which the DM coder can follow and it is called the maximum slope tracking capability of the D.M. system. If f_s is the sampling frequency then an input signal with slope exceeding $K.f_s$ gives rise to noise, known as the slope overload noise.

ii) Granular Noise: Under the situation when the slope of the input signal is such that the coder is able to track, the difference between the approximated signal and the actual signal is the granular noise.

The slope overload noise is dominant of the two types of noise when the step size is too small, whereas, the granular noise is more when the step size is too large.

4.4 Modified Delta Modulator:

In order to reduce the total noise one must optimize the step size. A fixed step size will not give an optimum performance in terms of the minimum output noise power. But, if the step size is varied in accordance with the instantaneous slope of the input signal, i.e., increase the step size under slope overload condition, we get a modified system which is referred to as the Modified Delta Modulator (MDM) in this thesis.

An MDM, with double step size during slope overload occurence and single step during nominal slope uses the following further encoding of binary digits to be transmitted.

i) Slope overload occurance and positive signal slope $\longrightarrow$ transmit 1 1

ii) Slope overload occurance and negative signal slope $\longrightarrow$ transmit 1 0

iii) No slope overload and positive signal slope transmit 0 1 - inplace of 1

iv) No slope overload and negative signal slope transmit 0 0 - inplace of 0

When slope overload occurs (i.e. first 'bit' of "two binary bit block" is 1) decoder at the receiver and chooses a double step to be added to the summer amplifier. On the other hand when there is no slope overload (i.e. first 'bit' of "two binary bit block' is '0') a single step is to be added to the summer amplifier. A summer amplifier followed by an integrator (similar to the 'integrator' in the local decoder) along with digital logic circuitry to sense properly the four code words transmitted forms the decoder.

We notice here that the bit rate (or the channel bandwidth) will have to be doubled compared to the bit rate of LDM transmitting just 'two' informations (i.e. whether '+ve slope' or '-ve slope') and having a constant step size. The performance of the MDM discussed above (with a bit rate of say R bits/sec) should be compared with the performance of LDM with 2 R bits/sec bit rate. This comparison has been done in Chapter V.

4.4.1 Coder Circuit:

Fig. 4.2 gives the block diagram of the MDM coder. The inputs to the Difference Amplifier (D.A.) are the input signal

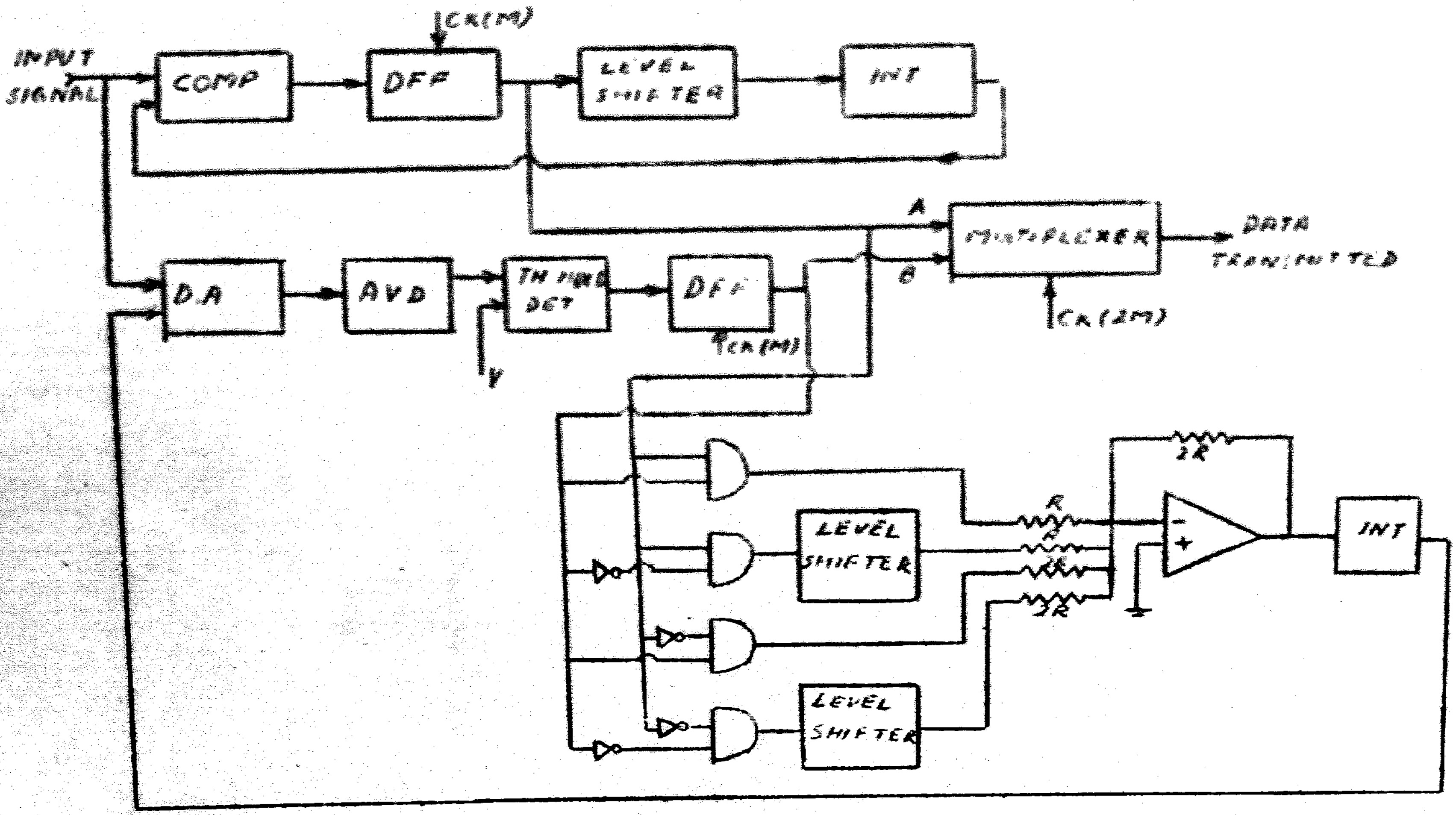

FIG. 4.2 BLOCK DIAGRAM - MDM CODER

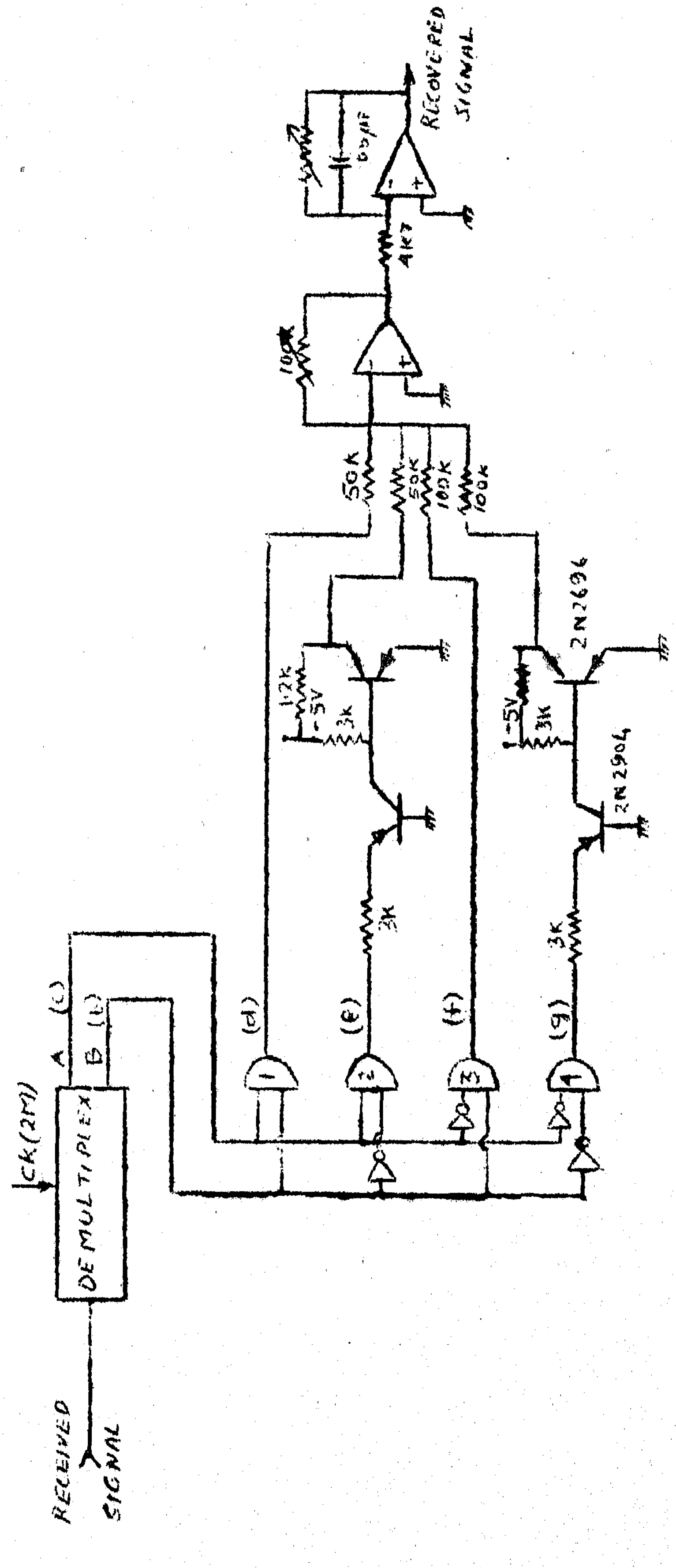

FIG. 4.3 MDM DECODER CIRCUIT

information) is available with only channel delay. Both these outputs give all the four informations (as discussed in the Sec. 4.4) required with the help of simple digital circuitry using 'AND' and 'INVERTER' gates as shown in the circuit diagram given in Fig. 4.3.

Fig. 4.4 explains how the four informations (d),(e), (f) and (g) (mentioned in Sec. 4.4) are obtained from the demultiplexer outputs A and B. Fig. 4.4(a) shows the input signal and the output of local decoder. Whenever the difference between these two signals increases more than the set voltage (say +v volts) e.g., at points P and Q, an "overload pulse" occurs (Fig. 4.4(b)). Duration of these overload pulses is determined by the period of time the difference voltage remains more than V volts. The "sign of slope" pulse (output A of demultiplexer) is shown in Fig. 4.4(c). From (b) and (c) other waveforms (d),(e),(f) and (g) are obtained with the use of simple gating. Before summing these pulses in the summer pulse trains (e) and (g) are level shifted from (0 to 5V) to (0 to -5V) as these pulse trains represent the -ve slope, waveform (h) shows the summed up waveform. Notice +ve and -ve slope overload pulses, viz, (d) and (e) are summed in the summer with a gain of 2. Integration of summed waveform (h) gives the recovered signal. The results obtained of modified delta modulator are discussed in Chapter V.

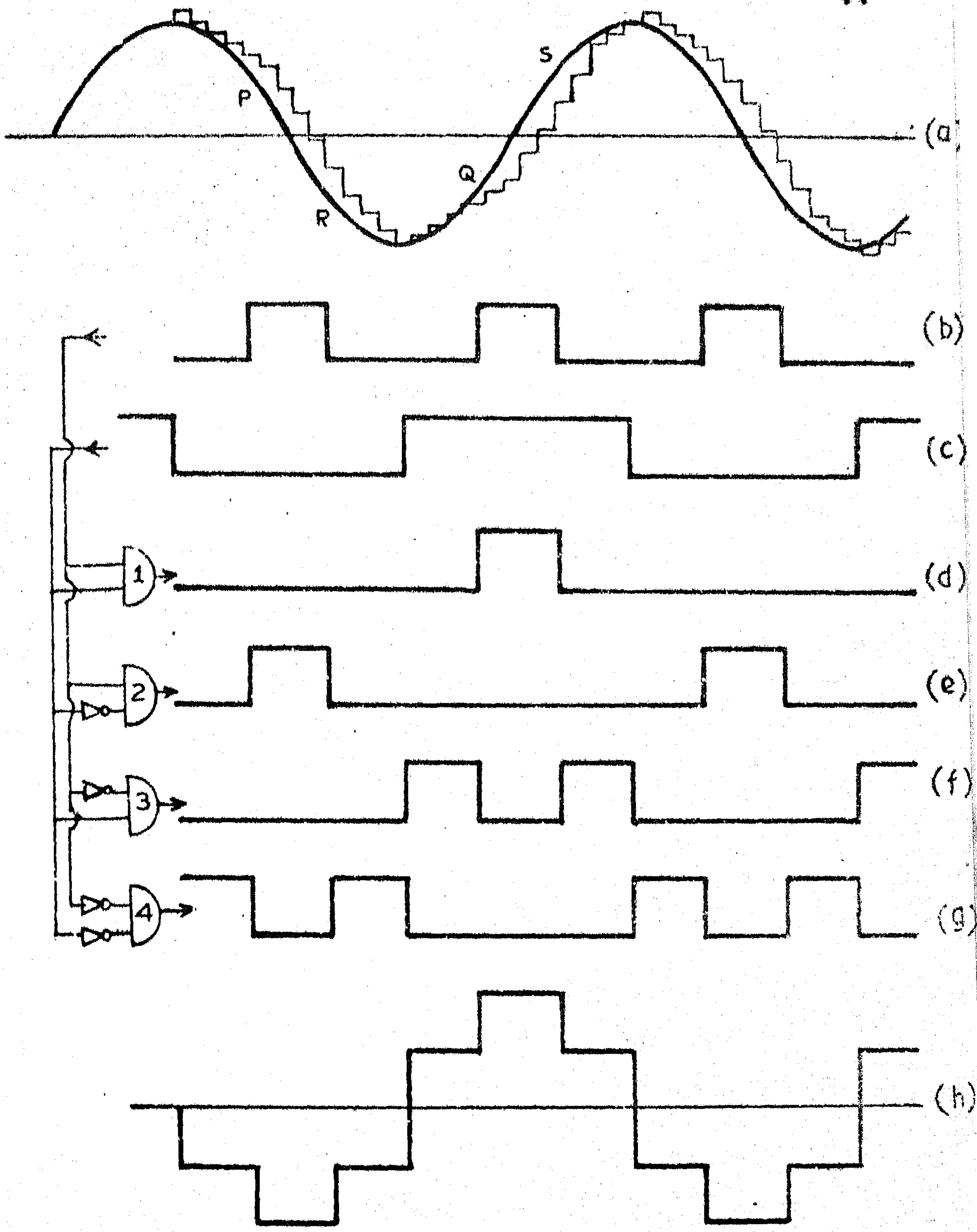

FIG. 4.4 WAVEFORMS AT DIFFERENT STAGES IN DECODER

CHAPTER V

CONCLUSIONS

5.1 Introduction:

To evaluate the performance of the fiber optic link two type of measuremnts viz. Bit Error Rate (BER) and Signal to Noise Ratio (SNR) were carried out. BER measurements were carried out in the "internal" and "external" modes - with and without line coding. Whereas SNR measurements were carried out in the 'internal' mode (using the internal 3 level line coding) along with source coding.

5.2 BIT Error Measurements:

Bit error rate (BER) measurements is divided in to the following parts;

i) BER measurement for the optical link only, i.e. using the optical transmitter (type HFBR 1001), the optical receiver (type HFBR 2001) and fiber optic cable (type HFBR 3003) in cascade without using any external line encoder/decoder, etc. Measurements were made for the following modes:

a) External mode (without any line coding)
b) Internal mode (with internal line coding)

ii) BER measurements using 1B-2B line encoder/decoder with a set up as shown in Fig. 5.1.

iii) BER measurements using 2B-3B line encoder/decoder with a set up as shown in Fig. 5.1.

Results obtained in the above measurements are tabulated in Table 5.1 and Table 5.2. Bit error rate versus bit rate

Table 5.1

External Mode (without any line coding)				Internal Mode (with provided internal line coding)			
Bit rate in Mbits/sec	Time in clock periods	Error Count	Bit Error rate	Bit rate in Mbits/sec	Time in clock periods	Error Count	Bit Error rate
1	10^9	0	$<10^{-9}$	1.00	10^9	0	$<10^{-9}$
2.0	10^9	0	$<10^{-9}$	2.00	10^9	0	$<10^{-9}$
2.5	10^9	0	$<10^{-9}$	3.00	10^9	0	$<10^{-9}$
2.94	10^8	24	2.4×10^{-7}	4.00	10^9	0	$<10^{-9}$
3.00	10^8	3900	3.9×10^{-5}	4.50	10^9	0	$<10^{-9}$
3.20	10^6	9400	9.4×10^{-3}	4.65	10^9	1	10^{-9}
3.47	10^5	8200	8.2×10^{-2}	4.80	10^8	2000	2×10^{-5}
				5.0	10^5	400	4.5×10^{-3}
				5.405	10^5	600	6×10^{-3}

Table 5.2

With 1B-2B Coding					With 2B-3B Coding				
Symbol rate in Mbits/sec	Bit rate in Mbits/sec	Time in Symbol clock periods	Symbol Error Count	Symbol Error Rate	Symbol rate in Mbits/sec	Bit rate in Mbits/sec	Time in symbol clock periods	Symbol Error Count	Symbol Error Rate
0.50	1.00	10^9	0	$<10^9$	0.666	1	10^9	0	$<10^{-9}$
1.00	2.00	10^9	0	$<10^9$	1.333	2	10^9	0	$<10^{-9}$
1.25	2.50	10^9	0	$<10^9$	1.8832	2.75	10^9	0	$<10^{-9}$
1.92	3.84	10^9	18	1.8×10^{-8}	1.946	2.92	10^9	0	$<10^{-9}$
1.95	3.90	10^6	1	1×10^{-6}	2.026	3.04	10^7	5	5×10^{-7}
1.98	3.96	10^4	27	2.7×10^{-3}	2.136	3.205	10^5	10	1×10^{-4}
2.083	4.166	10^5	7000	7×10^{-2}	2.22	3.33	10^5	45	4.5×10^{-4}
2.25	4.50	10^3	180	1.8×10^{-1}	2.381	3.5715	10^5	[illegible]	[illegible]

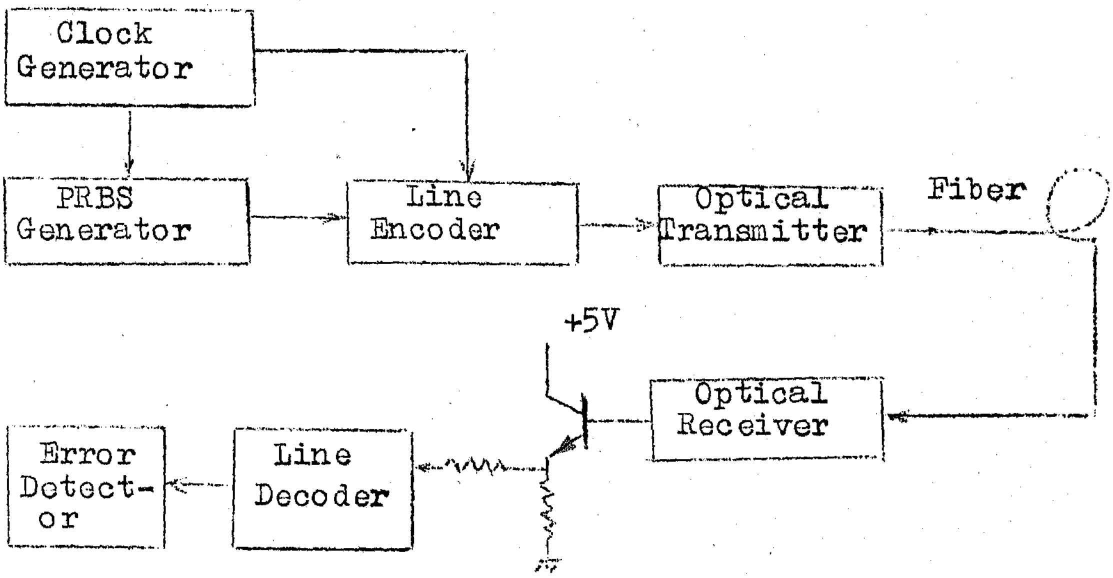

Fig. 5.1: Measurement set up for BER Measurement

plots for various measurements are shown in Fig. 5.2. Curves (a) and (b) of Fig. 5.2 correspond to the measurement set up of above mentioned graphs (i) (a) and (i)(b), respectively. While curves (c) and (d) of Fig. 5.2 correspond to the measurement set up of groups (ii) and (iii), respectively.

Pseudo Random Bit Sequences (PRBS) were generated which matched the internal sequences generated in the error detector (Type 3761A of Hewlett Packard Ltd.). The length of the PRBS is given by 2^N-1, where N was choosen as 15.

5.3 <u>Signal to Noise Ratio Measurement</u>:

Performance of source coder/decoder described in Chapter IV was evaluated through this measurements. Modified

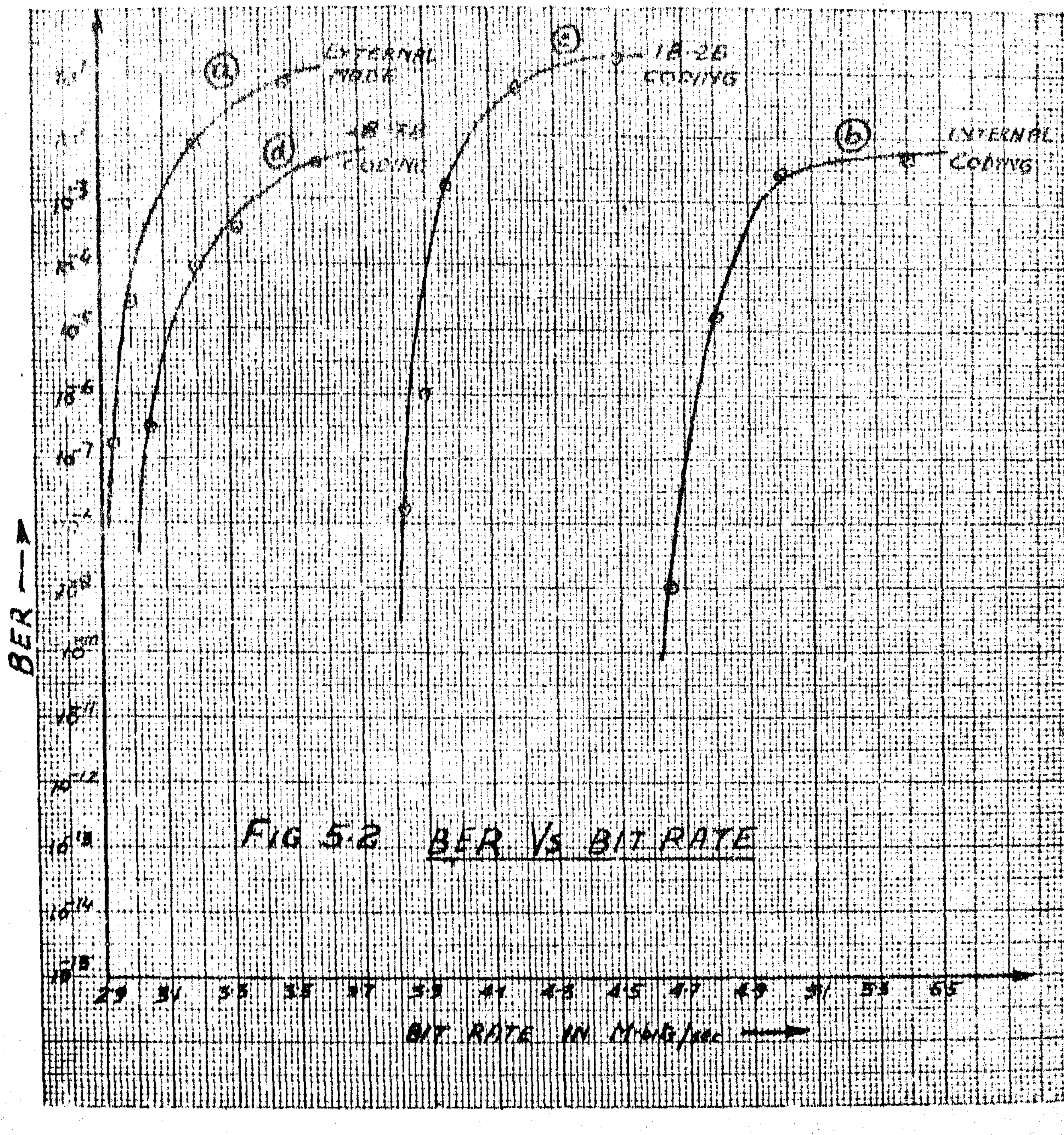

FIG 5.2 BER Vs BIT RATE

delta modulator (MDM) is used as the source coder along with the optical transmitter in the internal coding mode (three level optical flux coding scheme described in Chapter II). So the internal coder can be considered to be the line coder in this case. The SNR measurements were divided in the following four groups.

i) With Linear Delta Modulator (LDM) as source coder along with internal mode of optical transmitter.

ii) With modified delat modulator as source coder along with internal coding mode of optical transmitter.

iii) With LDM as source coder, but, without any line coding and optical channel.

iv) With MDM as source coder, but, without any line coding and optical channel.

Fig. 5.3 gives the set up used for above mentioned SNR measurements. SNR measurements were done with the help of a distortion analyzer (Type 330D of Hewlett Packard Company). Results of SNR measurements are tabulated in Table 5.3 and Table 5.4. These results are also plotted in Fig. 5.4, Fig. 5.5 and Fig. 5.6, respectively.

5.4 Conclusion:

It can be seen from curve (b) of Fig. 5.2 that the HP fibre optic link can be operated at a bit rate of

4.65 Mbits/sec with a BER of 10^{-9} when used in the "Internal Mode" only. From curve (a) of the figure it is seen that for the same BER a data rate of only 2.9 Mbits/sec can be achieved using the "External Mode" of operation. The pulse format in both the cases was RZ. So the manufacturer's

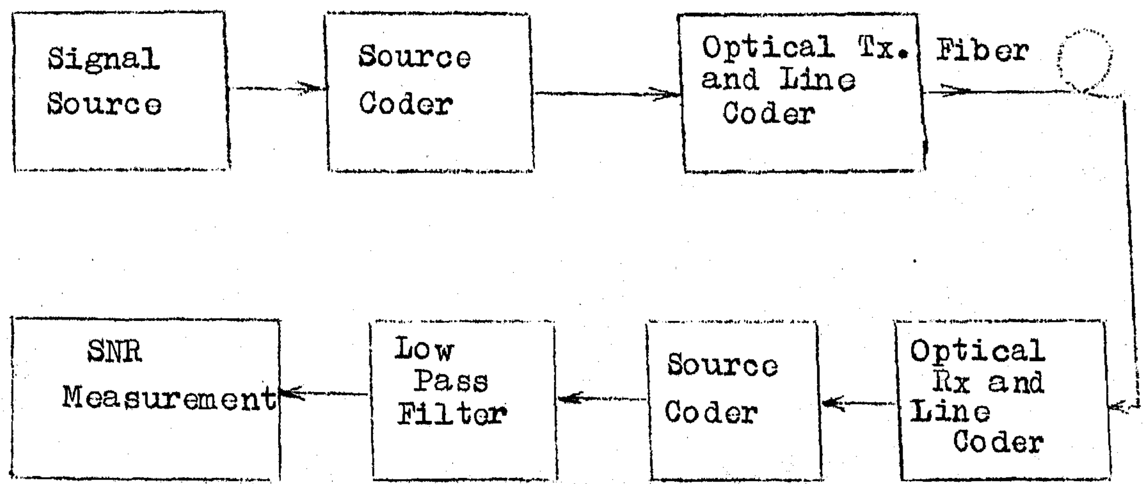

Fig. 5.3: SNR Measurement set up.

claim of obtaining a bit rate of 10 Mbits/sec. NRZ at a BER of 10^{-9} seems to be a little optimistic.

The role of line coding in improving the performance can be observed from curves (c) and (d) of Fig. 5.2. It can be seen that for the same BER of 10^{-9} the data rate improves to 3 Mbits/sec with 2B-3B coding and 3.82 Mbits/sec with 1B-2B line coding technique when the External Mode of operation was used. However, the three-level coding used

Table 5.3

Input signal frequency in KHz	Signal level = 0.38V and Optimum threshold			
	With Line Coding		Without Line Coding	
	SNR with LDM as source coder (dB)	SNR with MDM as source coder (dB)	SNR with LDM as source coder (dB)	SNR with MDM as source coder (dB)
0.5	26.5	28.0	26.5	28.0
1.0	26.0	29.0	26.0	29.0
1.5	26.0	29.0	26.0	29.0
2.0	24.0	27.5	24.0	27.5
2.5	21.5	25.0	21.0	25.0
3.0	18.0	20.0	18.0	20.0

Table 5.4

With LDM						With MDM					
at 0.5 KHz		at 1 KHz		at 2 KHz		at 0.5 KHz		at 1 KHz		at 2 KHz	
Signal level in dB	SNR dB	Signal level in dB	SNR dB	Signal level in dB	SNR dB	Signal level in dB	SNR dB	Signal level in dB	SNR dB	Signal level in dB	SNR dB
7.958	24	7.958	23.5	7.958	22.5	7.958	25.5	7.958	26.0	7.958	25.0
12.042	26.5	10.882	25.5	12.042	24.5	13.980	29.0	12.042	29.0	12.042	27.5
18.062	29.5	13.980	27.0	13.980	24	16.902	31.0	17.502	27.5	15.564	25.5
21.938	26.0	18.062	23.0	16.902	22	20.00	30.0	20.00	22.5	18.00	22.5
23.522	23.0	20.00	21.5	-	-	23.522	22.0	-	-	-	-

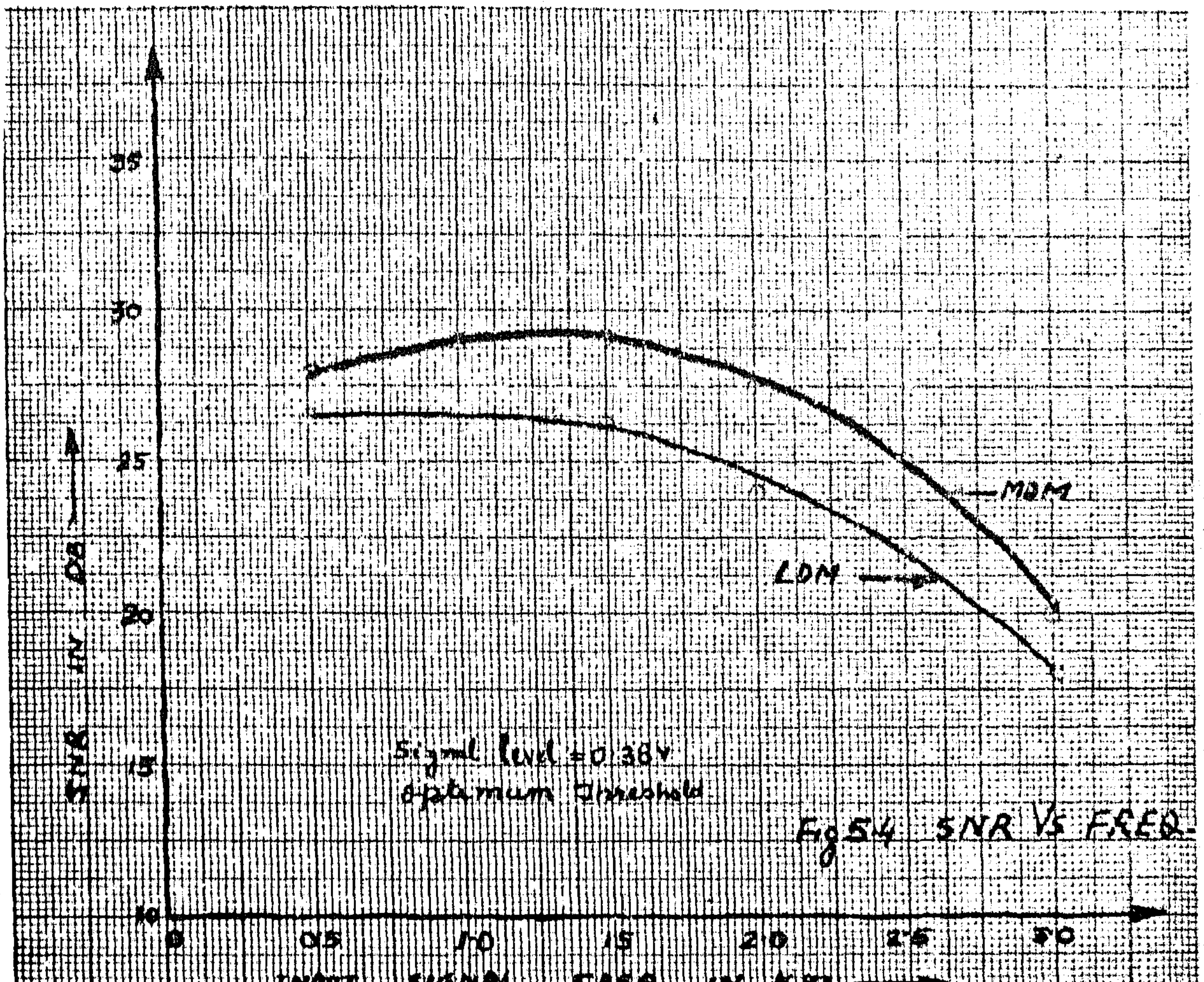

Fig 5.4 SNR Vs FREQ.

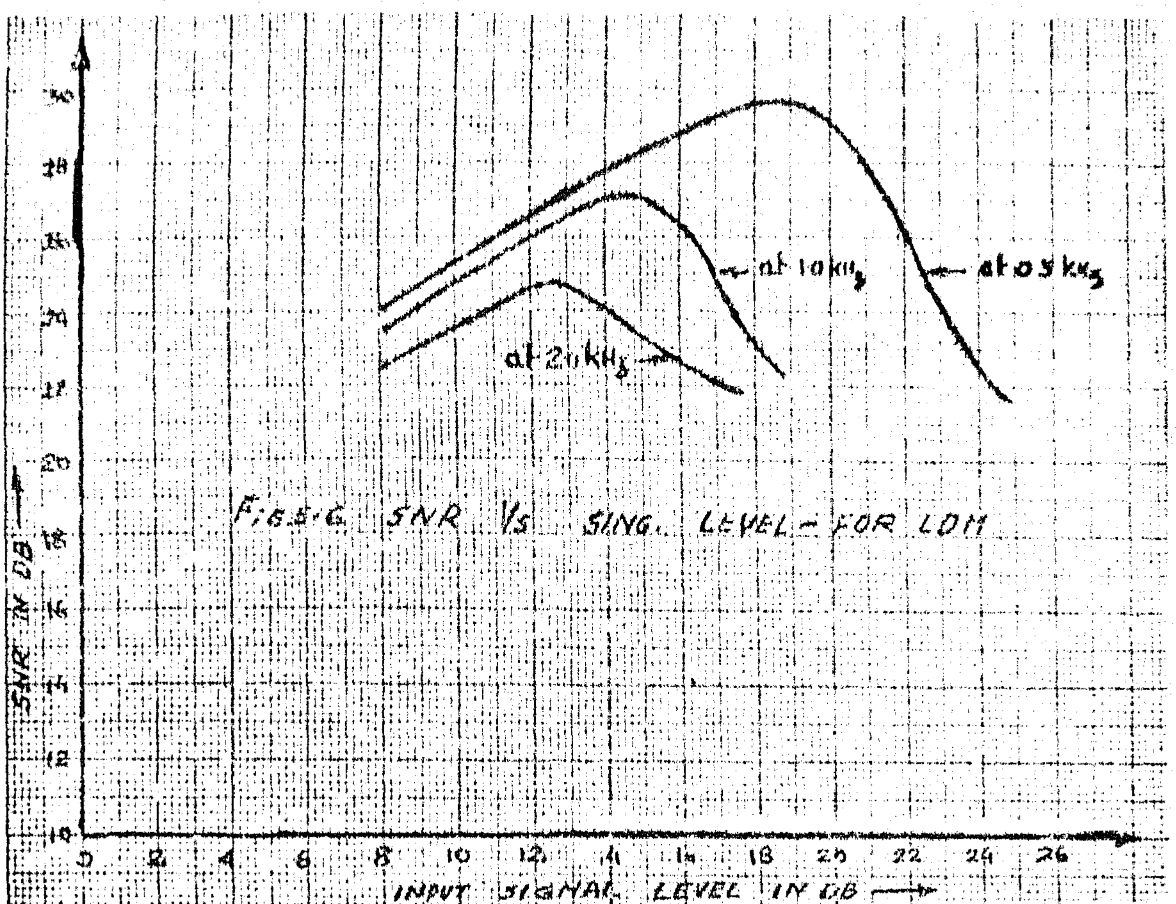

Fig. 5.6 SNR Vs SING. LEVEL - FOR LDM

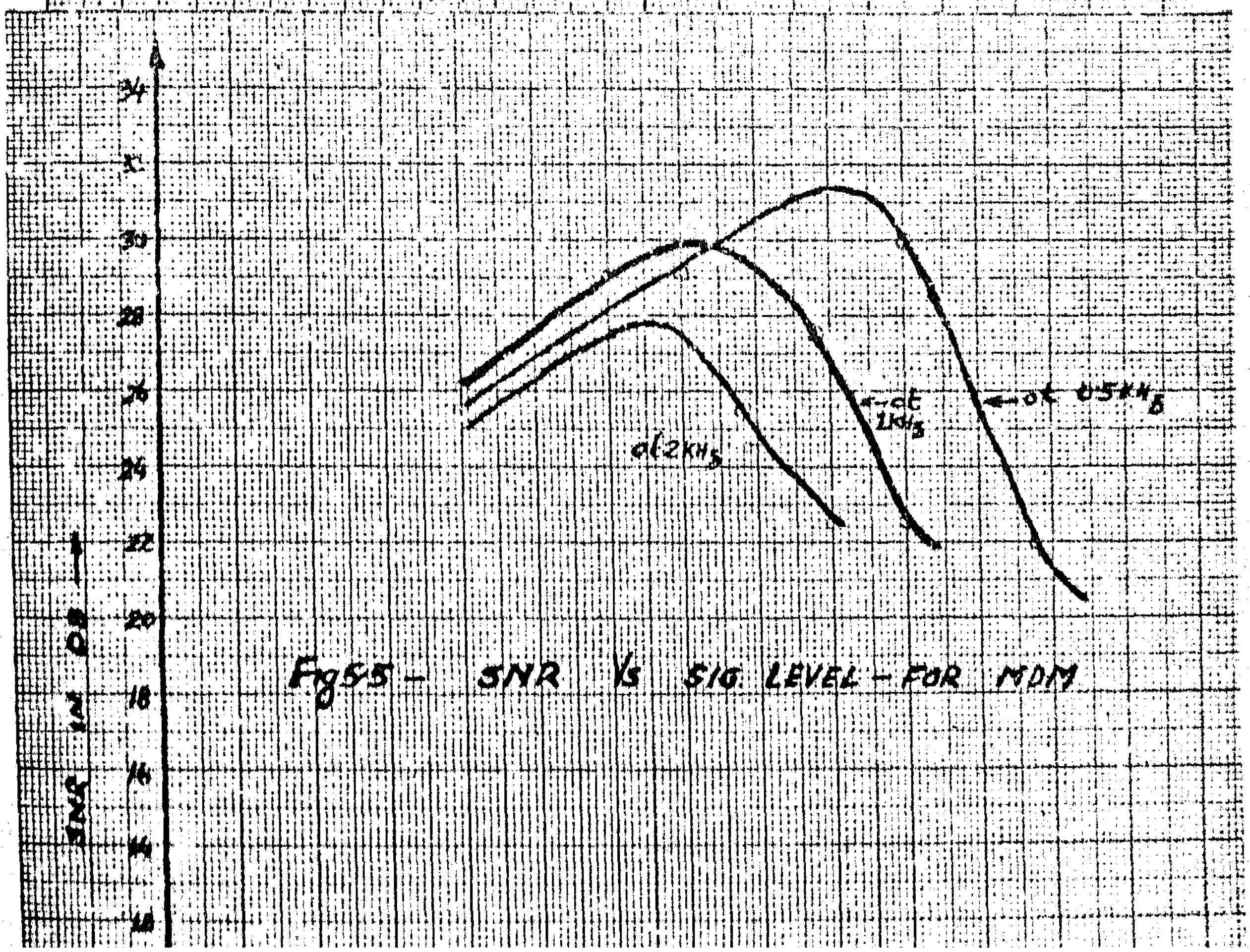

Fig 5.5 - SNR Vs SIG. LEVEL - FOR MDM

in the Internal Mode of operation is still much better. In this case, the flux excursion ratio K is exactly equal to one and full dynamic range of the front-end amplifier in the receiver is utilized giving a much better performance as is seen earlier. Similarly, the performance of 1B2B coding is better than 2B3B because of the reason that a flux excursion ratio nearer unity is achieved in the former case.

Performance of the linear delta modulator/demodulator does not change when used in conjunction with the optical fibre link. A peak SNR of 29.5 dB is obtained for a 0.5 KHz single tone input at a clock rate of 64 K bits/sec. The modified coder gives a peak SNR of 31.5 dB for the same input at the same transmission rate. Overall, the MDM is seen to give an improvement in SNR of 3 dB.

The source coders were used along with the Internal Mode operation of the fibre link. The External Mode operation of the link was not possible at such bit rates.

Further work in line encoding can be done in different directions. Higher order pulse formats like 3B4B, 5B6B, etc. can be experimented with. Correlatives decoding techniques in place of the conventional decoding can be used for further improvement in performance. More

sophisticated pulse formats have also been proposed by some people which can be used. The effective of more sophisticated line coding plans on the synchronization problems of the link should be examined.

The modified coder can be improved further by using more than one threshold levels, for overload situations. Moreover, for underload inputs reduction of the step size in a similar manner can be investigated.

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